HPCA-9

9th Annual International Symposium

on

High Performance Computer Architecture

Conference Program

http://www.cs.arizona.edu/hpca9

CROWNE PLAZA
ANAHEIM-GARDEN GROVE, CA
February 8 – 12, 2003

HPCA is supported by generous donations from Intel Corporation, IBM Corporation, California Institute for Telecommunications and Information Technology and The Henry Samueli School of Engineering at UCI.

TCCA

Workshops
Saturday, February 8, 2003
INTERACT-7: The 7th Annual Workshop on Interaction between Compilers and Computer Architectures Gyungho Lee , University of Illinois at Chicago Wei Hsu , University of Minnesota
SAN-2: 2nd Annual Workshop on Novel Uses of System Area Networks Mark Heinrich, Cornell University Evan Speight, Cornell University
NP-2: The Second Workshop On Network Processors Patrick Crowley, University of Washington Mark Franklin, Washington University in St. Louis Haldun Hadimioglu, Polytechnic University Peter Z. Onufryk, IDT (Starts 1:30pm)
Sunday, February 9, 2003
CAECW-02: Sixth Workshop on Computer Architecture Evaluation using Commercial Workloads Kimberly Keeton, Hewlett-Packard Laboratories Russell Clapp, Ashwini Nanda, IBM TJ Watson Research Center
NP-2: The Second Workshop On Network Processors Patrick Crowley, University of Washington Mark Franklin, Washington University in St. Louis Haldun Hadimioglu, Polytechnic University Peter Z. Onufryk, IDT
SSRS: Workshop on Software Support for Reconfigurable Systems Majid Sarrafzadeh, UCLA Computer Science Dept Ryan Kastner, UCSB ECE Dept

Tutorials	
February 8 8:30-12:30	An introduction to Network Processors Patrick Crowley, U. Washington
February 9 1:30-5:30	Simics Microarchitect's Toolset Peter Magnuson, Virtutech

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CONFERENCE PROGRAM

Sunday, February 9

Conference Reception (7:30 pm)
Made possible by Cal-(IT)2 and the HSSoE at UCI.

Monday, February 10

Welcome (8:45am – 9:00 am)

Keynote I (9:00am – 10:00 am)
Chair: Laxmi Bhuyan
Billion Transistor Chips in Mainstream Enterprise Platforms of the Future
Dileep Bhandarkar
Architect-at-Large, Enterprise Platforms Group, Intel Corporation

Break (10:00am-10:30am)

Session 1: Multithreading (10:30am - 12:00 n)
Chair: Antonio Gonzalez
Variability in Architectural Simulations of Multi-threaded Workloads, Alaa Alameldeen and David Wood
Mini-threads: Increasing TLP on Small-Scale SMT Processors, Joshua Redstone, Susan Eggers, and Henry Levy
Front-End Policies for Improved Issue Efficiency in SMT Processors, Ali El-Moursy and David Albonesi

Lunch (12:00n - 1:30pm)

Session 2: Branch Prediction (1:30pm - 3:00pm)
Chair: Susan Eggers
Reconsidering Complex Branch Predictors, Daniel Jimenez
Incorporating Predicate Information Into Branch Predictors, Beth Simon, Brad Calder, and Jeanne Ferrante
Dynamic Data Dependence Tracking and its Application to Branch Prediction, Lei Chen, Steve Dropsho, and David Albonesi

Break (3:00pm – 3:30pm)

Session 3: Power Efficient Designs (3:30pm - 5:30pm)
Chair: Saman Amarasinghe
Control Techniques to Eliminate Voltage Emergencies in High-Performance Processors, Russ Joseph, David Brooks, and Margaret Martonosi
Dynamic Voltage Scaling with Links for Power Optimization of Interconnection Networks, Li Shang, Li-Shiuan Peh, and Niraj Jha
Power-Aware Control Speculation through Selective Throttling, Juan L. Aragon, Jose Gonzalez, and Antonio Gonzalez
Deterministic Clock Gating For Microprocessor Power Reduction Hai Li, Swarup Bhunia, Yiran Chen, Kaushik Roy, and T.N. Vijaykumar

TCCA Meeting (5:30pm-6:30pm)

BANQUET (6:30pm)

Tuesday, February 11

Keynote II (8:30am - 9:30am)
Chair: Brad Calder
Beyond Performance: Some (other) Challenges for Future Microprocessors. *Eric Kronstadt, Director, VLSI Systems, IBM TJ Watson Research Center*

Break (9:30am - 10:00am)

Session 4: Superscalars (10:00am - 12:00n)
Chair: David Wood
Runahead Execution: An Alternative to Very Large Instruction Windows for Out-of-order Processors, Onur Mutlu, Jared Stark, Chris Wilkerson, and Yale Patt
Microarchitecture and Performance Analysis of a SPARC-V9 Microprocessor for Enterprise Server Systems, Mariko Sakamoto, Akira Katsuno, Alichiro Inoue, Takeo Asakawa, Haruhiko Ueno, and Kuniki Morita
Exploring the VLSI Scalability of Stream Processors, Brucek Khailany, William J. Dally, Scott Rixner, Ujval J. Kapasi, John Owens, and Brain Towles
Dynamic Optimization Of Micro-Operations, Brian Slechta, Brian Fahs, David Crowe, Michael Fertig, Gregory Muthler, Justin Quek Francesco Spadini, Sanjay J. Patel, and Steven S. Lumetta

Luncheon (12:00n - 1:30pm)

Session 5 Multiprocessor Systems (1:30pm - 3:00pm)
Chair: Chita Das
Slipstream Execution Mode for CMP-Based Multiprocessors, Khaled Ibrahim, Gregory Byrd, and Eric Rotenberg
Tradeoffs in Buffering Memory State for Thread-Level Speculation in Multiprocessors, Maria Garzaran, Milos Prvulovic, Victor Vinals, Jose Llaberia, Lawrence Rauchwerger, and Josep Torrellas
Dynamic Data Replication: An approach to Providing Fault-Tolerant Shared Memory Clusters, Rosalia Christodoulopoulou, Reza Azimi, and Angelos Bilas

Break (3:00pm – 3:30pm)

Session 6: Memory and Communication Performance (3:30pm - 5:30pm)
Chair: David Albonesi
Memory System Behavior of Java-Based Middleware, Martin Karlsson, Kevin Moore, Erik Hagersten, and David Wood
Evaluating the Impact of Communication Architecture on the Performability of Cluster-Based Services, Kiran Nagaraja, Neeraj Krishnan, Ricardo Bianchini, Richard Martin, and Thu Nguyen
Hierarchical Back-Off Lock for Non-Uniform Communication Architectures, Zoran Radovic and Erik Hagersten
Performance Enhancement Techniques for InfiniBand Architecture, Eun Jung Kim, Ki Hwan Yum, Chita Das, Mazin Yousif, and Jose Duato

Wednesday, February 12

Keynote III (8:00am - 9:00am)
Chair: Josep Torrellas
The State of State
Peter Kogge, McCourtney Professor of Computer Science and Engineering, University of Notre Dame

Session 7: Profiling and Simulation Support (9:00am - 10:00am)
Chair: Bill Mangione-Smith
Catching Accurate Profiles in Hardware, Satish Narayanasamy, Timothy Sherwood, Suleyman Sair, Brad Calder, and George Varghese
A Statistically Rigorous Approach for Improving Simulation Methodology, Joshua Yi, David Lilja, and Douglas Hawkins

Break (10:00am - 10:30am)

Session 8 10:30 am – 12:30 pm

8-A Caching and Prefetching
Chair: Soner Onder
Caches and Merkle Trees for Efficient Memory Authentication
Blaise Gassend, Ed Suh, Dwaine Clarke, Marten van Dijk, and Srinivas Devadas
Just Say No: Benefits of Early Cache Miss Determination, Gokhan Memik, Glenn Reinman, and William Mangione-Smith
TCP: Tag Correlating Prefetchers, Zhigang Hu, Stefanos Kaxiras, and Margaret Martonosi
Cost-sensitive Cache Replacement Algorithms, Jaeheon Jeong and Michel Dubois

8-B Networks and Communication
Chair: Qing Yang
Scalar Operand Networks, Michael Taylor, Walter Lee, Saman Amarasinghe, and Anant Agarwal
A Methodology for Designing Efficient On-Chip Interconnects on Well-Behaved Communication Patterns, Wai Hong Ho and Timothy Pinkston
Inter-cluster Communication Models for Clustered VLIW processors, Andrei Terechko, Erwan Le Thenaff, Manish Garg, Jos van Eijndhoven, and Henk Corporaal
Active I/O Switches in System Area Networks, Ming Hao and Mark Heinrich