

Billion Transistor Chips in Mainstream Enterprise Platforms of the Future

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Abstract

Today's leading edge microprocessors like the Intel's Itanium[®] 2 Processor feature over 220 million transistors in 0.18 μ m semiconductor process technology. Nanotechnology that continues to drive Moore's Law provides a doubling of the transistor density every two years. This indicates that a Billion transistor chip is possible in the 65 nm technology within the next 3 to 4 years. Such chips can be used in mainstream enterprise server platforms.

This talk will review the progress in semiconductor technology over the last 3 decades since the introduction of the first microprocessor in 1971. A short video tape will provide a historical perspective on Moore's Law in the form of an interview with co-founder Gordon Moore, and his thoughts for the future of semiconductor technology.

Key trends in high end microprocessor design including multi-threading and multi-core will be covered. We have started to see "SMP-on-a-chip" designs for high-end enterprise servers where two processors with Level 2 (L2) cache are incorporated on a single chip. Future microprocessors will offer higher levels of multiprocessor capability on chip as the transistor density increases.

Computer manufacturers are incorporating these high-end microprocessors into large symmetric multiprocessing systems with 8, 16, 32 or even 64 processors. Another trend is the emergence of clustered commercially off the shelf (COTS) servers as credible supercomputing platforms.

This talk will cover anticipated advances in semiconductor technology and relate those to trends in microprocessor design that will drive higher levels of parallelism in mainstream server platforms. Several possible ways of utilizing a billion transistors will be discussed along with accompanying design challenges.