DEVASHREE TRIPATHY

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PHD CANDIDATE IN COMPUTER SCIENCE

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SUMMARY

My interest lies in Computer Architecture, GPGPU Architecture design, Machine Learning, High Performance Computing, Fault-Tolerance systems. Recent highlights include:

- Building data-dependent programming support for GPUs and Big Data accelerators,
- Boosting GPU performance using the intelligent data-locality analysis,
- Smart power management techniques for Scientific and Big Data applications in high-performance computing systems.

EDUCATION

PhD in Computer Science (CGPA: 3.9/4.0)
UNIVERSITY OF CALIFORNIA, RIVERSIDE | Riverside, CA | 2015-Present

Master of Technology, Advanced Electronics Systems (CGPA: 8.53/10)
CSIR – CENTRAL ELECTRONICS ENGINEERING RESEARCH INSTITUTE | Pilani, India | 2014

Bachelor of Technology, Electronics and Telecommunications Engineering (CGPA: 9.69/10)
VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY (FORMERLY UCE) | BURLA, India | 2012

NOTABLE PROJECTS

PhD in Computer Science **2015-Present**

INTELLIGENT DATA LOCALITY EXTRACTION USING JUST IN TIME (JIT) COMPILER

- Employed the JIT compiler analysis to find the data-locality between structures at various granularity such as threads, warps (intra-core) and TBs (inter-core) in a GPU kernel.
- This information can help make smarter decisions for a locality aware data-partition and scheduling in multi-GPUs, as well as single GPUs.

PAVER: LOCALITY GRAPH-BASED THREAD BLOCK SCHEDULING FOR GPUS (TACO 2021)

- Design efficient Thread-Block (TB) scheduling policy by leveraging the inter-TB data locality information to reduce the L1 and L2 accesses.
- Used C++ to modify GPGPU-Sim.

GREENMM/ SAOU: ENERGY EFFICIENT GPU MATRIX MULTIPLICATION THROUGH UNDERVOLTING AND OVERCLOCKING (ICS, 2019, ISLPED 2020)

- Explored different errors and derived a fault model as a function of undervolting levels, overclocking frequency and data size.
- We operated the GPU beyond the minimum operating voltage and maximum operating frequency and correct the resulting faults using Algorithm-Based Fault Tolerance Technique (ABFT).
- Used CUDA and Nvidia System Management Interface to control the operating metrics.

SLUMBER: STATIC-POWER MANAGEMENT FOR GPGPU REGISTER FILES (ISLPED 2020)

- Explored the techniques to reduce leakage energy of the register files.
- We propose a hybrid energy saving technique where a combination of power-gating and under-volting is used to save optimum energy depending on the idle period of the registers.

REDESIGNING EFFICIENT FETCH UNITS IN GPGPUS

- Redesigned the GPGPU Fetch Units to eliminate the stalls caused in the pipeline due to the invalid instructions in the instruction buffers.
- Used C++ to modify GPGPU-Sim.

WIREFRAME: SUPPORTING DATA-DEPENDENT PARALLELISM THROUGH DEPENDENCY GRAPH EXECUTION IN GPUS (MICRO, 2017)

- Proposed and developed cross-stack software-hardware techniques to support data dependent parallelism in GPUs. Programmer-annotated and compiler-assisted technique generates a dependency graph to guide hardware scheduling and dependency resolution.
- Proposed new programming paradigm, programmer APIs, compiler analysis, and hardware scheduling techniques.
- Evaluated by modifying GPGPU-Sim simulator in C++ and modifying Nvidia CUDA benchmarks

LATENT SEMANTIC INDEXING USING NON-NEGATIVE MATRIX FACTORIZATION ON GPU

- Used CUDA to implement the iterative updates of NMF factorization
- Analyzed the effectiveness of NMF for extracting latent semantic information from TREC documents Dataset w.r.t SVD.

IMPLEMENTATION OF TWO-LEVEL ROUND ROBIN WARP SCHEDULING AND DYNAMIC WARPS ON GPGPU-SIM

- Used C++ to modify the source code of GPGPU-Sim, specifically its warp scheduling mechanism, for performance improvement.

Master of Technology, Advanced Electronics Systems **2012-2014**

PATIENT ASSISTANCE SYSTEM USING BRAIN COMPUTER INTERFACE (MTECH THESIS)

- Used MATLAB to create the BCI Application to detect and quantify the features of the brain signals which indicated the user's intentions and translated these features into device commands to accomplish the user's intent. The project achieved a classification accuracy of 96%.

OPTICAL CHARACTER RECOGNITION USING NEURAL NETWORKS

- Processed the scanned images using feature extraction techniques.
- Customized neural network Algorithm was used to obtain a classification accuracy of 90% of the extracted characters.

AN IMPROVED SOBEL EDGE DETECTION

- Used MATLAB to improve the sobel edge detection of the Noisy images using Wavelet Transform.

FINGERPRINT RECOGNITION USING GABOR FILTER

- Used VHDL to implement the fingerprint image enhancement module and Gabor filter on Virtex II Pro FPGA.

Bachelor of Technology, Electronics & Telecommunication Engineering **Sept – Dec 2011**

HOME APPLIANCE CONTROL USING SMS (DISSERTATION PROJECT)

- SIM 300 GSM Modem used to send text message(SMS) and enable serial communication with microcontroller (ATMEGA 128).

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NOTABLE PUBLICATIONS

Detailed list in google scholar.

Tripathy, Devashree, AmirAli Abdolrashidi, Laxmi Bhuyan, Liang Zhou and Daniel Wong, "PAVER: Locality Graph-based Thread Block Scheduling for GPUs" *ACM Transactions on Architecture and Code Optimization* **(TACO, 2021),** vol 18, issue 3, article 32, pp 1-26.

Tripathy, Devashree, Hadi Zamani, Debiprasanna Sahoo, Laxmi Narayan Bhuyan, and Manoranjan Satpathy "Slumber: Static-Power Management for GPGPU Register Files"
ACM/IEEE International Symposium on Low Power Electronics and Design **(ISLPED, 2020),** pp. 109-114, 2020.

Zamani, Hadi, **Devashree Tripathy,** Laxmi Bhuyan, and Zizhong Chen. "SAOU: Safe Adaptive Overclocking and Undervolting for Energy-Efficient GPU Computing" *ACM/IEEE International Symposium on Low Power Electronics and Design* **(ISLPED, 2020),** pp. 205-210, 2020.

Zamani, Hadi, Yuanlai Liu, **Devashree Tripathy**, Laxmi Bhuyan, and Zizhong Chen. "GreenMM: energy efficient GPU matrix multiplication through undervolting." In Proceedings *of the ACM International Conference on Supercomputing **(ICS 2019)***, pp. 308-318, 2019.

Das, Swagata, Devashree Tripathy, and Jagdish Lal Raheja. *Real-time BCI System Design to Control Arduino Based Speed Controllable Robot Using EEG*. Springer, 2018.

Abdolrashidi, AmirAli, **Devashree Tripathy**, Mehmet Esat Belviranli, Laxmi Narayan Bhuyan, and Daniel Wong. "Wireframe: Supporting data-dependent parallelism through dependency graph execution in gpus." In *Proceedings of the 50th Annual IEEE/ACM International Symposium on Microarchitecture **(MICRO 2017)***, pp. 600-611. 2017.

Tripathy, Devashree, and Jagdish Lal Raheja. "Design and implementation of brain computer interface-based robot motion control." In *Proceedings of the 3rd International Conference on Frontiers of Intelligent Computing: Theory and Applications (FICTA) 2014*, pp. 289-296. Springer, Cham, 2015.

COURSES MASTERED

- ✓ Computer Architecture
- ✓ GPU Architecture
- ✓ High Performance Computing
- ✓ Image Processing
- ✓ FPGA & Reconfigurable Systems
- ✓ Real-time Embedded Systems
- ✓ Operating System
- ✓ Data Mining
- ✓ Algorithms
- ✓ Compiler

SKILLS

Coding	C++ (Proficient)	Python (Proficient)	CUDA (Proficient)	VHDL (Familiar)	Assembly x86	HTML
Others	Linux	Visual Studio	LaTeX	Xilinx ISE	MATLAB	Synopsys Design Compiler

AWARDS & DISTINCTIONS

- Student Scholarship for Grace Hopper Celebration (2020).
- Student Travel Grant for ISCA 2019, HPDC 2019, CRA-W Grad Cohort 2018, MICRO 2017, CWWMCA 2017, NAS 2016.
- Student Volunteer Award ISCA 2018.
- Dean's Distinguished Fellowship, UCR (2015)
- Quick-Hire Fellowship by Government of India (2012 – 2014)
- **1st rank** among all B.Tech. (undergraduate) students of VSSUT, Burla (2012)
- 1st rank among all girls in freshmen year of VSSUT, Burla (2008)
- Top 0.1% among all the students in India, Central Board of Secondary Education (2006)