Homework 3 for CSE153 (Fall 2019)

Due: Nov 22, F

Instructions:

***** Be brief in your answers. You will be graded for correctness, not on the length of your answers.

* Make sure to write legibly. Incomprehensible writing will be assumed to be incorrect.

I. Consider the following segment table:

Segment	Base	Limit
0	800	600
1	1200	140
2	70	100
3	1350	880
4	2200	96

(a) Is the information in the segment table consistent? If there are possible errors that you identify, what will their implication be? (2 points)

(b) What will be the result of translating the following virtual addresses? (2 points)
(i) 4,90
(ii) 2,200

II. (a) An OS is using two-level paging to implement a 28-bit virtual address space per process. The page size is 256-bytes, and the machine does not have a TLB. Explain the steps involved in looking up the virtual address 0x03bf04d, when all pages are present in memory. Assume an even split of address bits between first- and second-level page tables. (2 points)

(b) For the system above, what is the maximum number of page faults that could be generated in response to a memory access? (2 points)

III. Consider a process that has been allocated 5 pages of memory: P1, P2, P3, P4, and P5. The process accesses these pages in the following order:

P1 P2 P3 P4 P1 P2 P5 P1 P2 P3 P4 P5

(i) Illustrate Belady's anomaly by precisely describing the execution of the FIFO page eviction algorithm in two cases: a) where the machine has 3 pages of physical memory, and b) where the machine has 4 pages of physical memory, and by comparing the number of page faults incurred in these two cases. (When the process begins executing, none of its pages are present in memory.) (2 points)

(ii) Show how the LRU page eviction algorithm would work in the same scenarios a) and b) described above. (2 points)