1. Implement the function

\[ F = a' b c + a b' \]

using only 3-input NAND gates and inverters. (5 points)

**Answer:**

![Logic Diagram]

(This is the logic diagram for the function using NAND gates.)
2. Given the following 1-minterms and d-minterms for four literals \( w, x, y, z \), determine (a) the PI list, (b) the EPI list, and (c) all the minimal covers. (10 points)

1-minterms: 1, 2, 3, 5, 6, 8

\( d \)-minterms: 10, 11, 14

**Answer:**

\[
\begin{array}{cccc}
00 & 0 & 1 & 1 & 1 \\
01 & 4 & 5 & 7 & 6 \\
11 & 12 & 13 & 15 & 14 \\
10 & 8 & 9 & 11 & 10 \\
\end{array}
\]

(a) PI list: \( w'y'z, yz', x'z', x'y \)

(b) EPI list: \( w'y'z, yz', w'x'z', x'y \)

(c) cover list:

\( w'y'z, yz', w'x'z', x'y \)
3. Implement a 2-to-1 mux using only AND, OR, and NOT gates. (5 points)

**Answer:**

![2-to-1 Mux Diagram]
4. Implement the function $F = x'b + x'y + yb$ using at least one 3-to-8 decoder. (5 points)

Answer:
5. Use a $4 \times 8 \times 4$ PLA to implement the following two functions. (5 points)

\[
y = M S_1' S_0' b + M S_1' S_0 b' + M S_1 S_0'
\]

and

\[
c = M S_1' S_0 + S_1' S_0' b
\]

**Answer:**

2 points for the connections in the AND array
2 points for the connections in the OR array
1 point for the connections in the output array