The M320C50 is a high-performance 16-bit digital signal processor with separate data and program memory. The central ALU has a 32-bit arithmetic logic unit, a 16-bit scaling shifter, and a 16 x 16 parallel multiplier. A separate parallel logic unit performs bit manipulations on any data memory location or control/status register. It uses a four stage instruction pipeline for speed of operation.

Peripherals are controlled through 28 memory-mapped registers and include: a timer, a serial port, a time-division-multiplexed serial port, a programmable wait-state generator, an interrupt controller and the I/O ports, 16 of which are memory mapped.

**Key Features**
- Software compatible with the TI 320C50, 320C51, 320C52 and 320C53
- 32-bit ALU/accumulator
- 16-bit parallel logic unit
- Up to 64K words each of program memory and data memory
- 64K I/O space
- Instruction times fully compatible with industry standard 320C50
- Two circular buffers
- Interrupt controller
- TDM serial port
- Programmable wait-state generator
- Fully synthesizable

**Deliverables**
- Verilog & VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL test benches
- Reference technology netlist
**MEMORY PROVISION**
The M320C50 contains no RAM or ROM but provides functional interconnect signals for connecting three dual-port RAM blocks (two 512x16, one 32x16); a program RAM or ROM block of up to 32Kx16 and up to 16 single-port data RAM blocks up to a total of 32Kx16.

**PROGRAM MEMORY**: The M320C50 supports up to 64K words of program memory, which can be formed from a combination of up to 32K words of internal (on-chip) program memory, internal single-port RAM, and external program memory. In addition, a 256x16 block of internal data RAM may be configured as program memory.

**DATA MEMORY**: The M320C50 supports up to 64K words of data memory, which can be formed from a combination of up to 32K words of internal dual-port and single-port RAM, and external data memory.

The external data memory can be of three types: ‘Local’; I/O selected; and ‘Global’. Local memory is exclusive to the M320C50 but Global memory can be shared with other devices, allowing cooperative processing with other digital signal processors.

**DESIGN FEATURES**

**CLOCK**: The M320C50 uses a single clock input which is divided by two internally to provide the instruction cycle clock. There is no divide-by-one mode.

**INTERNAL MEMORY SIZE**: The size of the internal program memory and internal single-port RAM are configurable, in units of 1K words, up to a maximum of 32K words each. The size of the individual RAM blocks used to form the single-port RAM is also configurable.

**POWER-DOWN MODES**: The M320C50 supports two power-down modes: a power-down of the core CPU only (leaving peripherals running), and a complete power-down of the core CPU and peripherals. A CPU Core power-down can be exited by any interrupt. A complete power-down mode can be exited by an external interrupt.

**REFERENCE TECHNOLOGY GATE COUNT**: 40000

**SIGNAL DESCRIPTION**
The M320C50 has 55 DSP inputs and 79 DSP outputs, plus 238 functional interconnect signals that allow the end user to choose the appropriate memory blocks for each implementation and to configure internal program memory as RAM.

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AI[14:0]</td>
<td>Input</td>
<td>Address bus inputs, used during DMA</td>
</tr>
<tr>
<td>DI[15:0]</td>
<td>Input</td>
<td>Data bus inputs</td>
</tr>
<tr>
<td>READY</td>
<td>Input</td>
<td>Data ready</td>
</tr>
<tr>
<td>NRD, NWR</td>
<td>Output</td>
<td>External memory read/write cycle indicator</td>
</tr>
<tr>
<td>NDS, NRS</td>
<td>Output</td>
<td>Data memory/Program memory select</td>
</tr>
<tr>
<td>NIS</td>
<td>Output</td>
<td>I/O select</td>
</tr>
<tr>
<td>NRD</td>
<td>Output</td>
<td>Data bus direction indicator for external bus</td>
</tr>
<tr>
<td>NSTRBO</td>
<td>Output</td>
<td>External bus cycle strobe</td>
</tr>
<tr>
<td>NHR, NWR</td>
<td>Output</td>
<td>External memory read/write cycle indicator</td>
</tr>
<tr>
<td>NBR</td>
<td>Output</td>
<td>Bus request to access global memory</td>
</tr>
<tr>
<td>NIAQ</td>
<td>Output</td>
<td>Instruction acquisition</td>
</tr>
<tr>
<td>NHEDA</td>
<td>Output</td>
<td>Hold acknowledge</td>
</tr>
<tr>
<td>NACK</td>
<td>Output</td>
<td>Interrupt acknowledge</td>
</tr>
<tr>
<td>XF</td>
<td>Output</td>
<td>External flag output</td>
</tr>
<tr>
<td>CLKO</td>
<td>Output</td>
<td>Instruction cycle clock output</td>
</tr>
<tr>
<td>NHOE</td>
<td>Output</td>
<td>3-state enable control signal</td>
</tr>
<tr>
<td>TOUT</td>
<td>Output</td>
<td>Timer output</td>
</tr>
<tr>
<td>DX</td>
<td>Output</td>
<td>Serial port transmit data output (+Enable)</td>
</tr>
<tr>
<td>TDX</td>
<td>Output</td>
<td>Serial port transmit data output (+Enable)</td>
</tr>
<tr>
<td>CLKXO</td>
<td>Output</td>
<td>Serial port transmit clock output (+Enable)</td>
</tr>
<tr>
<td>TCLKXO</td>
<td>Output</td>
<td>Serial port transmit clock output (+Enable)</td>
</tr>
<tr>
<td>TADD</td>
<td>Output</td>
<td>Serial port address output (+Enable)</td>
</tr>
<tr>
<td>FSXO</td>
<td>Output</td>
<td>Serial port frame synch output (+Enable)</td>
</tr>
<tr>
<td>TFXSO</td>
<td>Output</td>
<td>Serial port TX frame synch (+Enable)</td>
</tr>
<tr>
<td>IDLE2</td>
<td>Output</td>
<td>Idle2 mode indicator</td>
</tr>
</tbody>
</table>

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