International Technology Roadmap for Semiconductors
1999 Edition

System-on-a-Chip

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SYSTEM-ON-A-CHIP

Historically, the Roadmap has emphasized the technological limits of silicon production, leading to the specification of the most complex chips that can be developed in the categories of memory, microprocessor, and ASIC at a particular technology node. With the growing importance of high-volume consumer markets and the ability to integrate almost all aspects of a system design on a single chip, the ITRS has included an additional vehicle to capture the requirements of this important, emerging area. This vehicle is referred to as a System-On-a-Chip (SoC, sometimes called System LSI). Two classes of SoC can be distinguished by applications: the *mainstream, cost-driven* SoC (C-SoC) targeted towards high-volume consumer markets, and the *high-end, performance-oriented* SoC (P-SoC), targeted towards lower-volume, high-performance markets. The primary differences between these categories are illustrated in Table 8.

Table 8 Major Characteristics and Emphasis of SoC Classifications

CHARACTERISTIC	*C-SOC MAINSTREAM SOC*	*P-SOC HIGH-END SOC (FORMERLY ASIC)*
Major Drivers	Low-cost, low-power	Performance, complexity
Power	Lowest possible	Upper technological limits
Package	Very low cost	High-performance, expensive
Pins–I/Os	Few	Many

WHAT IS A SYSTEM-ON-A-CHIP?

There are a number of characteristics that distinguish an SoC, but the main consideration is that it is primarily defined by its cost rather than by technological limits. Rather than asking, "How complex a chip can I build?" and then asking, "How much will it cost?" (the P-SoC emphasis), in the C-SoC category the question most often asked is, "If my budget for this component is $N, how much capability (gates, memory, performance, and so on) can I expect to get?" The answer to this question is a complex combination of many factors. If one assumes a high-volume consumer part and so ignores nonrecurring engineering (NRE) costs related to design, then production costs include the fundamental technological factors contemplated in the ITRS (feature size, yield, field size, metal layers) as well as such factors as the cost of packaging and the cost of testing the SoC.

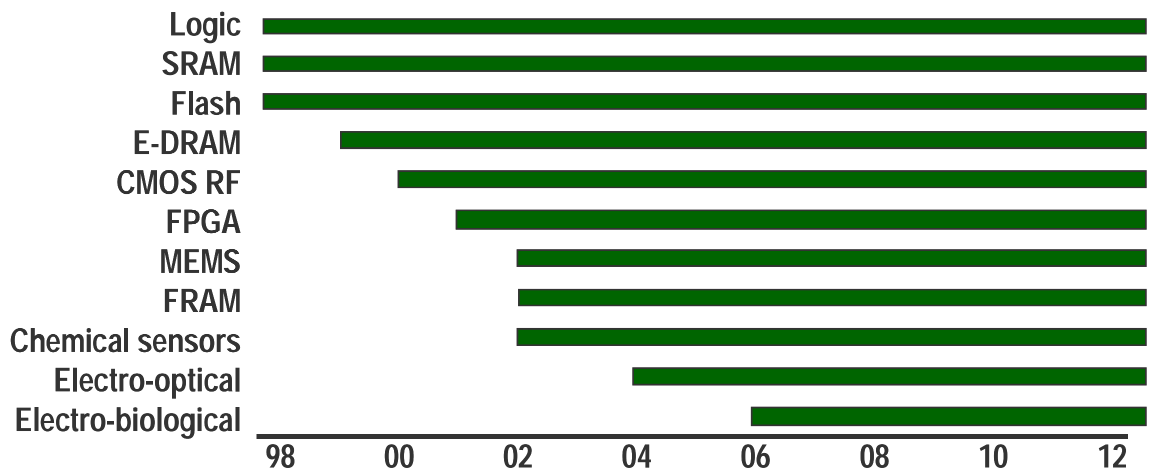

Figure 1 Technologies Integrated on SoC in the Standard CMOS Process

SoCs are also distinguished by other factors. As a *system*-on-a-chip, they are often mixed-technology designs, including such diverse combinations as embedded DRAM, high-performance or low-power logic, analog, radio frequency (RF), and even more esoteric technologies like Micro-electro Mechanical Systems (MEMS) and optical input/output.

In all categories of the Roadmap, design productivity is a key requirement. Design reuse will grow as a major tool in achieving the productivity requirements. This is particularly true for the SoC category, where time-to-market for a particular application-specific capability is a key requirement of the designs. The building blocks combined to form the SoC may be a controller core, embedded SRAM memory, and some dedicated logic. In some cases specific components/technological features may be added such as embedded Flash, embedded DRAM, MEMS, chemical sensors, or ferroelectric RAM (FRAM). The particular expectations for such mixed technologies are included in Figure 1. The number of such additional technological features on a specific SoC is likely to be limited to one or two for cost reasons.

For SoC, it is imperative that any additional technologies like those listed in Figure 1 be integrated into the standard CMOS logic process. Thus, process modules are needed that have little interference with the rest of the process and can be selected or de-selected freely depending on the application.

MAIN EMPHASIS—COST-BASED DESIGNS

The major new suggested emphasis of the SoC category is the C-SoC cost-based design.

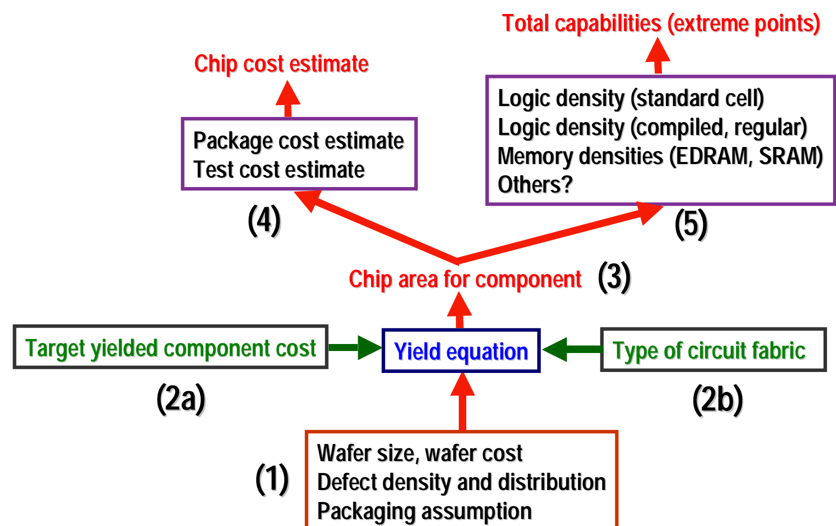

Figure 2 Possible Flow for Estimation of New Roadmap Entries

Given the nonlinear relationship between chip area and yielded die for a given technology node, as well as the post-processing yield enhancement techniques available for certain fabrics (such as DRAM repair), it is not as simple as determining a cost-per-mm^2 and then multiplying by chip area. For these reasons, we have approached the problem as outlined in Figure 2. Based on raw manufacturing data (1) and yield considerations for a particular class of circuit (2b), it is possible to predict the maximum yielded die area (3) of a particular class of circuit for given cost (2a). Given the likely I/O requirements and performance requirements of the circuit, package and test costs can be predicted, based on empirical data and projected new technology capabilities (4). Also predictable are required upper bounds for these aspects of the design, given a desire to maintain packaging and test at a particular percentage of overall chip cost (5).

Process technology is only one consideration that determines the cost-per-unit functionality of a particular family of circuits. Issues such as post-manufacture repair, test requirements, and binning play an important role in determining final cost. For a given process node, different circuit-styles, which have particular

functional density and yields, are known as particular *circuit fabrics*. Table 9 contains a partial list of such fabrics, some of which have reasonable cost models. However, some cost models are either not available or remain a difficult research problem to determine.

Table 9 Example of Circuit Fabrics

Circuit Fabrics
Hand-designed static CMOS logic
Standard-cell auto place and route logic
Regular logic structures (datapath)
Dynamic CMOS logic
SRAM
Embedded DRAM
Integrated CMOS analog
Integrated CMOS RF circuits
Processor cores

There are many factors for each fabric that effect cost. The most well-defined aspect of analysis, based on data already present in the ITRS, is the expected manufacturing cost for a particular size of chip and for a particular class of circuit (fabric). This data is projected in the ITRS for DRAM, hand-crafted logic, and auto-placed-and-routed logic—the circuit fabrics that have approximate cost projections, as shown in Figure 3.

Using this information, along with the memory and logic density numbers in the ITRS Overall Technology Characteristics tables, it is possible to estimate the capabilities of such a chip for various combinations of logic and memory.

From this information, a series of plots for each technology node of the form shown in Figure 3 could be developed.

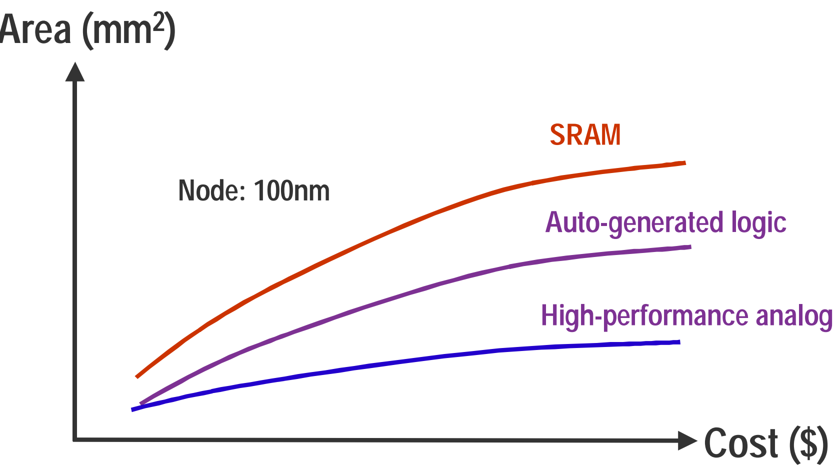

Figure 3 Schematic Representation of Area-cost Curves for Particular Circuit Fabrics at a Technology Node

PROGRAMMABLE VERSUS HARD-WIRED

Another factor to be considered in the context of this new SoC category is that of programmability (via software or programming gates, as in an field programmable gate array (FPGA)). The SoC provides a useful vehicle for introducing the notion of embedded software and its implications in the Roadmap. This aspect is of particular importance for design and test, as the methodological implications of a programmable versus nonprogrammable (hard-wired) implementation of an SoC are very significant. In the consumer marketplace, as well as in the high-performance ASIC markets, there are legitimate reasons for employing

both approaches, having to do with extreme points of performance, cost, and power dissipation. Some example applications in each category are listed in Table 10 to illustrate the point.

Table 10 Example Applications of Programmable and Nonprogrammable SoCs

	PROGRAMMABLE	*NON-PROGRAMMABLE*
C-SoC	Low-cost PDA chip Digital camera chip FPGA Microcontroller-based SoC	Sensor interface Low-cost home RF front end
P-SoC	High-end game platform Set-top box High-end network router DSP	Read-channel for disc drive High-performance network chip

PROCESS REQUIREMENTS FOR ADVANCED TECHNOLOGIES

It is expected that SoC will continue to use a number of exotic circuit fabrics, including those listed in Table 9 and some of the technologies listed in Figure 1. It will require the integration of technologies that are not part of the basic CMOS flow. In all cases, the goal should be to add additional steps to the CMOS process to incorporate these additional capabilities without altering the basic CMOS flow. The designer will then be able to choose the additional fabrics needed (such as RF and Flash memory) and estimate their impact on overall chip cost, performance, reliability, and power without disturbing the basic cost of the standard CMOS portion of the chip.

Examples of specific technologies that might be developed to support the integration of these mixed circuit fabrics include the following:

- Special wiring and metallization for high-performance analog and RF
- Special upper-layer processes and passivation for integrated MEMS
- Special localized processing for integrated optical sensors
- Use of discretionary implants for critical low-power regions of a chip (such as dual threshold)

Other process adjustments may be necessary and may be identified in the future.

The process complexity will be a major factor in the cost of the SoC applications. The more combinations of technologies that are assembled on a single chip, the more complex the processing will be. The total cost of processing will be hard to predict for these new materials and combinations of processing steps but an attempt at estimating this is shown in Table 11.

Table 11 shows an estimate of the increasing complexity of the new combinations of technologies in the units of extra lithography mask levels necessary to add this technology to the standard CMOS logic technology. The data in this table illustrates that the embedded additions of technologies add significant processing complexity and are compounded as the technologies are added together. The addition of more than two embedded technologies would increase the complexity incrementally.

Table 11 Added Process Complexity for SoC Technologies

Cost of adding technology in units of mask levels	Logic	SRAM	Flash	DRAM	CMOS RF	FPGA	MEMS	FRAM	Chemical Sensors	Electro Optical
Logic	0									
SRAM	1–2	0								
Flash	4	3–4	0							
DRAM	4–5	3–4	7–9	0						
CMOS RF	3–5	5–9	6–9	6–10	0					
FPGA	2	2–4	4–6	3–7	5–7	0				
MEMS	2–10	3–12	6–14	6–15	5–15	4–12	0			
FRAM	4–5	3–4	7–9	2–3	7–10	6–7	9–15	0		
Chemical Sensors	2–6	3–7	6–10	6–11	5–11	4–8	4–16	6–11	0	
Electro-Optical	5–8	6–9	9–12	9–13	8–12	7–10	7–18	9–13	7–14	0

PACKAGING CONSIDERATIONS

SoC designs will require a wide range of packaging solutions and will be responsible for driving many aspects of the packaging industry from low-cost, low pincount packages for C-SoC, to high-performance, high pincount packages for P-SoC. In addition, the mix of technologies, from analog and RF to optical and even MEMS devices will require a broad range of special packaging options. Some of the issues in each of these areas are discussed in this section.

SYSTEM-ON-A-CHIP PACKAGING

The ever-increasing CMOS density is a very important driving force for SoC in low-cost and hand-held applications. For example, when the lithography feature size improves in the succeeding generation, the chip size of a standalone micro-controller core may be limited by the pad pitch and pad count, and will not reduce accordingly. Very often, the combination of a controller core plus a digital signal processor (DSP) core may result in a chip I/O count less than either the controller or the DSP core alone and may still fit in such an I/O pad-limited chip area. The cost of two packages is replaced by one of equal or less cost (the package cost becomes less than one half), and the printed wiring board area being occupied is reduced. This also eliminates many of the off-chip driver circuits and the associated delay time and power consumption. Furthermore, the availability of on-chip wiring may allow substantial increase in the data bandwidth between these two cores, thus improving the performance. Similar benefit may also be achieved by the integration of A/D and D/A converters into the DSP and controller cores after one more technology generation. In some applications, programmability is essential, which may be achieved by a small embedded-Flash memory.

The main challenges in SoC packaging are in maintaining signal integrity and verification. Techniques like de-coupling, shielding, and better grounding will be necessary to handle mixed analog and digital signals in a minimum size package. Design emulation and verification of intent will require early packaging involvement in SoC design. The complexity of testing at both the wafer probe and package levels should be considered at the design stage.

In some applications, the chip size is not limited by the I/O pads, even when it should decrease in the succeeding generation. The reduction in chip size will decrease the chip cost. The integration of two cores into one chip may impact the chip yield and increase the overall chip cost. The replacement of two packages by one of equal or less I/O leads may cut the packaging cost by more than a factor of two. The cost of chip plus package may decrease or increase, depending on the individual application. However, the elimination of the off-chip driver delay and power consumption, the reduction in the wiring board area, and the

possibility of improved bandwidth between the two cores, may become important considerations for the adoption of the performance-oriented SoC applications.

RF AND MIXED-SIGNAL PACKAGING

The challenges in this area will become important as low-cost mobile and high bandwidth products drive across several market segments. The increasing performance of silicon ICs will enable lower cost solutions in the frequency domain below 10GHz. GaAs ICs, and now SiGe ICs will be used for higher frequency or higher power applications. Signal integrity and cost issues become dominant. Flip chip attachment to package and embedded passives on the package will be key enabling technologies to package level performance. Low inductance and high-density packages like fine pitch ball grid array (FBGA)/chip scale packaging (CSP) will enable designers to use lower cost partitioning solutions than the traditional ceramic modules.

Integrated modeling and simulation tools are required to decrease design cycle time to acceptable levels. Performance, physical size, and cost driven integration will continue to arrive at a single chip radio that combines memory, processor, and mixed-signal functions, as discussed above. Fast design cycle time and accurate simulation at both the chip and package levels are enablers of this integration. High-speed test and higher level of functional test at the package level also become development challenges. MEMS will be used in the fabrication of filter, switch, oscillator, and other components in the next 2–4 years. They offer the benefit of small size, low insertion loss, low power consumption, integration with ICs, and the potential of low cost with batch fabrication. Reliability, potential temperature sensitivity, and hermetic/vacuum packaging of MEMS devices are key development challenges.

MULTI-CHIP PACKAGES, MULTI-CHIP MODULES, AND SYSTEM-IN-A-PACKAGE

The production volumes of multi-chip modules (MCMs) have lagged behind expectations in the marketplace but tracked the acceptance of the flip chip bump technology by the system houses. However, few-chip modules (2–3 chips) are in volume production, and by extending the definition of multi-chip packages (MCPs) to include RF and mixed-signal products, it is now expected that 4–5 chips (or more complex) modules will be common in the next few years. The MCP is often referred to as a system-in-a-package (SiP), which primarily addresses time-to-market needs for mixed-technology, highly-complex systems. As the SoC becomes feasible both technically and economically, the number of ICs on an MCP will most likely be reduced to realize both product cost and size gains.

For certain limited volume, high-performance products the system packaging technology of choice will still be classical (complex) MCMs because they provide the best cost and performance package solution. Very often, tens of logic and memory chips with high I/O lead count are placed at close proximity to minimize the time-of-flight delay between chips. In fact, the wiring capacity needed to implement such systems on ceramic MCMs is one order of magnitude larger than the plastic MCM technology can support today. The important considerations are the overall system cost, the system performance needs, and the reliability of the CMOS based system, not just the cost of the packaging alone. Because the DCA for extremely high I/Os is available for ceramic MCMs now, and is expected for plastic-based MCMs in the future, the whole system can be packaged in a very small area that still permits the lowering of the junction temperature through standard refrigeration techniques. This capability increases the reliability of the CMOS chips by 3–5 times and the performance of the CMOS chips by up to 15%. Since the drive for better system reliability is expected to increase in the future, the extended used of MCMs in the system design will follow.

In general, MCP/MCM/SiP will be driven by densification and cost reduction for low end C-SoC products, and by densification and performance for high end P-SoC products. Flip-chip technology will soon be used pervasively for MCP/MCM/SiP technology (whether few-chip MCP or classical MCM) so that enabling solutions for flip-chip technology (such as underfill) become among the key enabling solutions for MCP/MCM/SiPs as well. Other critical, enabling solutions for MCP/MCM/SiPs include:

- Special physical design tools that facilitate performance-driven place-and-route for simple or complex MCP/MCM/SiPs

- High density substrate and metallization technology
- Low-cost, available known good die (KGD). Chip reworkability and module testing will be major factors in determining the feasible complexity of multi-chip modules.

TEST FOR SOC

Historically, IC testing has been performed by automatic test equipment (ATE) that applied external stimulate to devices under test (DUTs) followed by observation of the response that was compared with stored expected results. The ATE were either purely digital, or they also contained analog instruments that were synchronized to the digital. Recently, a number of ATE manufacturers have begun selling "SoC testers" that are capable of testing DUTs containing digital, analog, memory, and RF elements; however, the tests are all externally applied.

It is becoming clear that if SoCs are ultimately implemented as a collection of heterogeneous circuit fabrics (from analog and RF to high-performance logic and memory), it will be necessary for test methodologies to be developed specific to a particular fabric and integrated into the fabric design flow. In other words, from a performance perspective and a cost perspective, an on-board form of test is essential. This prediction is also evident in the *Test* chapter of the ITRS, where it is predicted that traditional test methods will give way to ATE that stimulate testing circuits designed within the DUT. In the *Test* chapter, a low-cost ATE is described that is able to load digital SCAN chains within a DUT and observe the result. This digital tester has roughly 64-signal pins plus hundreds of lower-performance pins that simply observe whether or not most of the DUT pins can actively swing between 1 and 0 states. Built-in-self-test (BIST) is also being used to test embedded memory, but the art of BIST for analog or RF circuits is still in its infancy.

If the SoC is programmable, or contains a controller of some form, it is most likely that an hierarchical form of test will be employed in future systems. The programmable component will test itself and then be responsible for the coordinated testing of the other on-chip subsystems, possibly via some form of BIST in the component itself. Both performance issues as well as cost issues will motivate the final choices.

Table 12 on SoC Test technology requirements highlights six areas where solutions must be pursued or there are no know solutions for solving the complex testing issues that are arising with SoCs. These are as follows:

- New fault models will be required to handle crosstalk and new failure modes that will result from multi-level metal structures. The "stuck-at" single fault model is becoming less effective for computing expected test results for complex SoC fabrics.
- New test methods involving BIST are required that will allow low-speed, low-cost ATE to test the digital portions of SoCs at high speed.
- New Design for Testability techniques are required for analog testing, higher-level behavioral testing and others.
- BIST techniques must be developed to include memory testing with self-repair for redundant configurations, repair of logic circuits, analog, and others.
- Standards must be developed for test programming languages, test data, and fault models so that test reuse is possible to shorten SoC test development time.
- Test costs must be reduced through test time reduction, faulty chip repair, and new failure analysis techniques.

Table 12a SoC Test Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Fault Model							
Stuck-at fault model	Single fault	Single fault	Single fault	Single fault	Single fault	Single fault	Single fault
Delay fault model	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay
New fault model (crosstalk and others)			XX	XX	XX	XX	XX
New fault model (RT level fault model)				XX	XX	XX	XX
Test Method							
Low cost test technique for embedded DRAM (BIST + direct access)		XX	XX	XX	XX	XX	XX
High speed test using low speed tester (BIST with on chip clock generator, test circuit on tester board)			XX	XX	XX	XX	XX
Test technique for asynchronous circuit			XX	XX	XX	XX	XX
Crosstalk test			XX	XX	XX	XX	XX
Test strategy for IP core-based design (test control integration, test scheduling)			XX	XX	XX	XX	XX
Whole chip path delay test				XX	XX	XX	XX
IDDQ test for low-Vth circuit				XX	XX	XX	XX
Low power consumption test technique (test pattern adjustment, test scheduling)				XX	XX	XX	XX
ATPG for interleave at-speed tester				XX	XX	XX	XX
Self diagnostic technique on maximum frequency							XX
DFT							
DFT at gate level design (scan design)	XX	XX	XX	XX	XX	XX	XX
DFT at RTL design (DFT, testability analysis, overhead estimate)	XX	XX	XX	XX	XX	XX	XX
DFT at RTL design (fault simulator, ATPG)				XX	XX	XX	XX
DFT at higher level design (behavior level, hardware/software co-design)							XX
DFT at higher level design (high level synthesis with testability analysis)							XX
DFT for analog / mixed-signal	Block isolation test	Block isolation test	BIST, JTAG	BIST, JTAG	BIST, JTAG	BIST, JTAG	BIST, JTAG
Test integration (IP core isolation test)	XX	XX					
Test integration (test integration tool supporting cost-, area-, speed- and power-driven DFT selection)			XX	XX			
Test integration (fully automated cost-, area, speed- and power-driven test integration tool)					XX	XX	XX
DFT circuits generation (memory BIST, logic BIST, JTAG)	XX	XX	XX	XX	XX	XX	XX
At-speed test with low speed tester			XX	XX	XX	XX	XX

XX—applicable node years

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

Table 12a SoC Test Technology Requirements—Near Term (continued)

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
BIST							
Embedded memory BIST	Restricted use	Restricted use	Practical use	Practical use	Practical use	Practical use	Practical use
Embedded memory BIST (redundant configuration, self repair, many kinds of test algorithm)			XX	XX	XX	XX	XX
Logic BIST	Restricted use	Restricted use	Practical use for stuck-at faults	Practical use for stuck-at faults	Practical use for stuck-at faults	Practical use for stuck-at faults	Practical use for stuck-at faults
Logic BIST (high fault coverage, at-speed test on system operation, test time restraint, low power, low area overhead)			XX	XX	XX	XX	XX
Logic BIST (faulty chip repair)			XX	XX	XX	XX	XX
Analog/mixed-signal BIST			Restricted use (PLL, ADC)	Restricted Use (PLL, ADC)	Restricted Use (PLL, ADC)	Restricted Use (PLL, ADC)	Restricted Use (PLL, ADC)
Others							
Standardization							
Test data	WGL, VCD, STIL	WGL, VCD, STIL	STIL on EDA/ATE	STIL on EDA/ATE	STIL on EDA/ATE	STIL on EDA/ATE	STIL on EDA/ATE
Test method/test interface	P1500	P1500	P1500 on IP core/ EDA	P1500 on IP core/ EDA	P1500 on IP core/ EDA	P1500 on IP core/ EDA	P1500 on IP core/ EDA
Fault model/fault coverage	Stuck-at model	Stuck-at model	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage
Test Cost							
Test time reduction (full-scan IDDQ)	XX	XX					
Test time reduction (IP core-based design)			XX	XX	XX	XX	XX
Faulty chip repair (memory BISR)			XX	XX	XX	XX	XX
Faulty chip repair (logic BISR and others)							
Failure Analysis							
Electron beam tester	XX	XX					
Chip backside analysis	XX	XX	XX				
Design/package for backside analysis				XX	XX	XX	XX
Integrated failure analysis environments				XX	XX	XX	XX
Test generation for failure analysis				XX	XX	XX	XX
Failure analysis for analog circuits							XX
BIST pattern exchange technique							XX

XX—applicable node years

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

Table 12b SoC Test Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Fault Model			
Stuck-at fault model	Single fault	Single fault	Single fault
Delay fault model	Gate/path delay	Gate/path delay	Gate/path delay
New fault model (crosstalk and others)	XX	XX	XX
New fault model (RT level fault model)	XX	XX	XX
Test Method			
Low cost test technique for embedded DRAM (BIST + direct access)	XX	XX	XX
High speed test using low speed tester (BIST with on chip clock generator, test circuit on tester board)	XX	XX	XX
Test technique for asynchronous circuit	XX	XX	XX
Crosstalk test	XX	XX	XX
Test strategy for IP core-based design (test control integration, test scheduling)	XX	XX	XX
Whole chip path delay test	XX	XX	XX
IDDQ test for low-Vth circuit	XX	XX	XX
Low power consumption test technique (test pattern adjustment, test scheduling)	XX	XX	XX
ATPG for interleave at-speed tester	XX	XX	XX
Self diagnostic technique on maximum frequency	XX	XX	XX
DFT			
DFT at gate level design (scan design)	XX	XX	XX
DFT at RTL design (DFT, testability analysis, overhead estimate)	XX	XX	XX
DFT at RTL design (fault simulator, ATPG)	XX	XX	XX
DFT at higher level design (behavior level, Hardware/software co-design)	XX	XX	XX
DFT at higher level design (high level synthesis with testability analysis)	XX	XX	XX
DFT for analog / mixed-signal	BIST, JTAG	BIST, JTAG	BIST, JTAG
Test integration (IP core isolation test)			
Test integration (test integration tool supporting cost-, area-, speed- and power-driven DFT selection)			
Test integration (fully automated cost-, area-, speed- and power-driven test integration tool)	XX	XX	XX
DFT circuits generation (memory BIST, logic BIST, JTAG)	XX	XX	XX
At-speed test with low speed tester	XX	XX	XX

XX—applicable node years

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 12b SoC Test Technology Requirements—Long Term (continued)

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
BIST			
Embedded memory BIST	Practical use	Practical use	Practical use
Embedded memory BIST (redundant configuration, self repair, many kinds of test algorithm)	XX	XX	XX
Logic BIST	Extension of handling fault model	Extension of handling fault model	Extension of handling fault model
Logic BIST (high fault coverage, at-speed test on system operation, test time restraint, low power, low area overhead)	XX	XX	XX
Logic BIST (faulty chip repair)	XX	XX	XX
Analog/mixed-signal BIST	Total use	Total use	Total use
Others	Tester on chip	Tester on chip	Tester on chip
Standardization			
Test data	Analog data	Analog data	Analog data
Test method/test interface	Automated SoC test integration	Automated SoC test integration	Automated SoC test integration
Fault model/fault coverage	New standard fault model, its coverage	New standard fault model, its coverage	New standard fault model, its coverage
Test Cost			
Test time reduction (full-scan IDDQ)			
Test time reduction (IP core-based design)	XX	XX	XX
Faulty chip repair (memory BISR)	XX	XX	XX
Faulty chip repair (logic BISR and others)	XX	XX	XX
Failure Analysis			
Electron beam tester			
Chip backside analysis			
Design/package for backside analysis	XX	XX	XX
Integrated failure analysis environments	XX	XX	XX
Test generation for failure analysis	XX	XX	XX
Failure analysis for analog circuits	XX	XX	XX
BIST pattern exchange technique	XX	XX	XX

XX—applicable node years

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)