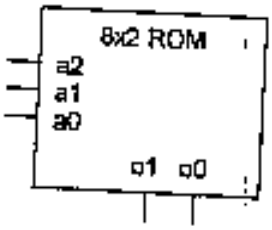
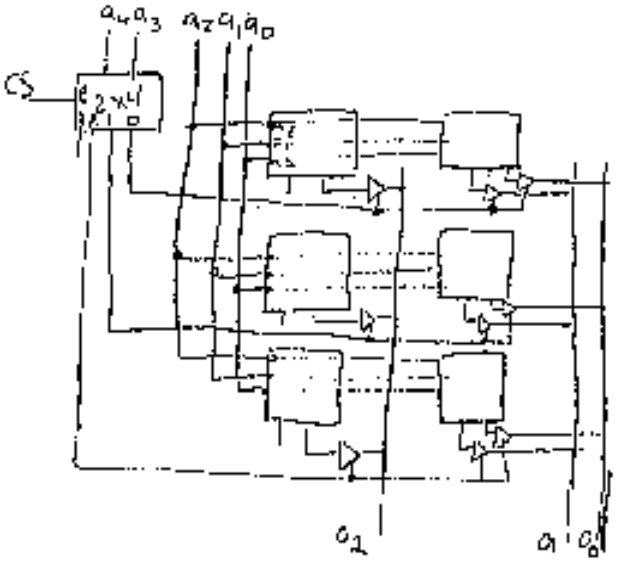
c) (8 points) Using a datapath. Provide the control word for each of the following desired operations, using the datapath of Fig 7.26 of Gajski's book (provided), using a minimum number of cycles, up to two. If an operation can't be done in two cycles, write "can't be done" under the Your Operations column, and leave the rest of that row blank. You *must* make maximum use of don't cares. *Make NO assumptions* about the prior contents of the registers. Registers are named R0 through R7. The instructions below are completely independent of one another. Remember that the register file's read ports output 0's when disabled.

Desired operation	Your operations (each one cycle only)	IE	WA			WE	RAA			REA	RAB			REB	ALU op. M S1 S0			Shifter op. S2 S1 S0			OE
		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R1 = R0 + 1	R1=R0+1	0	0	0	1	1	0	0	0	1	X	X	X	X	1	1	1	0	0	X	0
R2 = 16*R3	R2=shl(R3+R3); R2=shl(R2+R2)	0	0	1	0	1	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0
	also ok: shl(2*R3) or 4*R2	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	1	0	0	0
R7 = R7 / 2	R7=shr(R7+0) many other ways to get R7 through ALU	0	1	1	1	1	1	1	1	1	X	X	X	0	1	0	1	0	0	X	0
Inport = R6	can't be done																				

3) (6 points) Connecting memories. Below is a block diagram of an 8x 2 ROM, without chip select. But we need a 24x3 ROM with chip select. Show how to connect the 8x2 ROM's to create a 24x3 with chip select. Do not group wires – draw every wire distinctly, and label each wire clearly. You may use additional components, like decoders, multiplexors, tri-state buffers, gates, etc., but be sure to minimize your design.