CS161 – Fall 2016
Homework Assignment 2

Due: Tuesday, October 25th @ 11:59pm

Notes:

1- You are required to solve 2 questions out of 4 ☺

2- No late submissions (will not be graded)

practice-singlecycle.pdf can be accessed here: http://www.cs.ucr.edu/~kkhas001/practice-singlecycle.pdf
practice-multicycle.pdf can be accessed here: http://www.cs.ucr.edu/~kkhas001/practice-multicycle.pdf

1. Consider a change to the single-cycle processor that replaces the LOAD instructions with the pair of new instructions in the following way:

```
Original code:  LOAD    R1, R2, #100   /*R1=mem[R2+100] */

New code:       ADD     R4, R2, #100   /* R4=R2+100 */
                LOAD    R1, R4         /*R1=mem[R4] */
```

   Answer the following questions:

   a) What is the advantage of such code modification?

   b) What is the disadvantage of such code modification?

   c) Assume that the datapath components have the following delays: ALU – 2 nsec, register file read – 1 nsec, instruction memory – 2 nsec, data memory – 2 nsec. You can ignore all other delays and also assume that register file and memory write delays are not accounted for separately. Assume that LOAD instructions account for 30% of all instructions in the program. Would this modification result in a performance improvement or degradation? Explain.

   d) For the datapath component delays as presented in part (c), determine the maximum percentage of LOAD instructions in a program, so that the proposed modification still has a positive impact on performance. Explain.

2. Describe the modifications needed for a single-cycle datapath and control logic to support the execution of SLL (shift left logical) MIPS instructions. Add any necessary datapaths and control signals to the single-cycle datapath in practice-singlecycle.pdf and show the necessary additions to control signals Table in practice-singlecycle.pdf. Hint: Shift can be done using ALU. Operation of (ssl rt, rs, shamt) is (R[rt] = R[rs] << shamt).

3. In this exercise we examine in detail how an instruction is executed in a single-cycle datapath (use practice-singlecycle.pdf). Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word:

   10101100011000100000000000010100

   Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	-1	2	-3	-4	10	6	8	2	-16

   a) What are the values of the ALU control unit's inputs for this instruction?

   b) What is the new PC address after this instruction is executed?

   c) For each Mux, show the values of its data output during the execution of this instruction and these register values.

   d) For the ALU and the two add units, what are their data input values?

   e) What are the values of all inputs for the "Registers" unit?

4. Suppose that we wish to add support for four-operand arithmetic instructions to the **multi-cycle** datapath. An example of such an instruction is add3, which adds three numbers together instead of two:

   add3 R5, R6, R7, R8 /* R5=R6+R7+R8 */

   Assume that the instruction set is modified by introducing a new instruction format similar to the R-format except that bits [0-4] are used to specify the additional register (we still use rs, rt, and rd) and of course the new opcode is used. Describe the modifications needed for the datapath and control logic in practice-multicycle.pdf to support such instruction. *Your solution should not rely on adding extra read ports to the register file, nor should a new ALU be used.* Don't worry about the opcode decoding - concentrate on the operand fetch and execution logic. Indicate how many cycles will be required for this instruction.