

CS162 Homework 2  
Spring 2006

Name: \_\_\_\_\_

ID: \_\_\_\_\_

In the following eight-stage pipeline:

IF	DE	RR	EX1	EX2	MEM1	MEM2	WB
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where decode is split into two stages Decode (DE) and Register Read (RR) and both the Execute and Memory Access stages each take two stages (i.e., all ALU operations take two cycles, and the results are produced at the end of second stage of course). Assuming that forwarding is present, how many cycles would the machine need to stall when a loaded value is used in the immediate next instruction? Explain.