

# CS203A Fall 2004

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## Quiz 2

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Name \_\_\_\_\_

### Short questions

What are the advantages of Tomasulo algorithm over the Scoreboarding mechanism (4pts)?

- Avoids WAR and WAW hazards
- Decentralized vs. centralized control
- Hardware renaming, operands buffering
- Can execute programs beyond loops (dynamic loop unrolling)
- Prevents register file as a bottleneck
- Load/store disambiguation
- Supports forwarding through CDB

For the following code fragment, check all the instructions that can be put into the branch delay slot and explain why others cannot using one sentence (4ts).

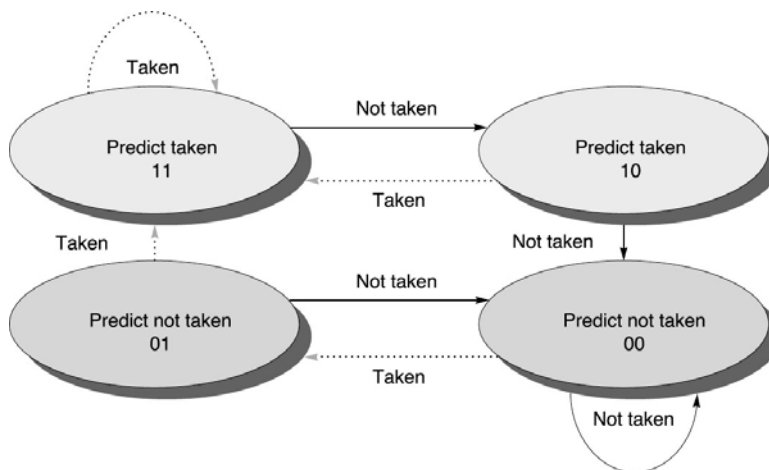
```
ADD  R1, R2, R3   no, BEQZ depends on R1
BEQZ R1, foo
branch delay slot
AND  R9, R1, R4   yes
OR   R7, R8, R9   no, OR depends on AND
foo: SUBD R4, R5, R6 no, will introduce wrong dependence between SUBD
and AND
```

Assume we use the 2-bit branch predictor shown below in a (2, 2) branch correlation prediction to predict the outcome of a branch.

Suppose the entry in the (2, 2) table shows

01	10	10	00
----	----	----	----

The global history register is 01. What is the prediction of the current branch (2pts)?



predict taken

**Scoreboarding (5pts):**

What is the instruction status table of the following code sequence:

```
MUL.D    F0, F6, F4
SUB.D    F8, F0, F2
ADD.D    F2, F10, F2
```

Assume that the MUL.D requires 3 clock cycles to execute and the SUB.D and ADD.D each takes 1 cycle to execute. Further, the processor has two add function units and one multiplier.

		ISSUE	OR	EX	WB
MUL.D	F0, F6, F4	1	2	3-5	6
SUB.D	F8, F0, F2	2	7	8	9
ADD.D	F2, F10, F2	3	4	5	8

If you allow data forwarding to happen in the register file:

		ISSUE	OR	EX	WB
MUL.D	F0, F6, F4	1	2	3-5	6
SUB.D	F8, F0, F2	2	6	7	8
ADD.D	F2, F10, F2	3	4	5	7