

# Lecture 7 Tomasulo's Algorithm

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## Review: Scoreboard

- Limitations of 6600 scoreboard
  - No forwarding
  - Limited to instructions in basic block (small *window*)
  - Number of functional units (structural hazards)
  - Stall on WAR hazards
  - Stall on WAW hazards



## Another Dynamic Algorithm: Tomasulo Algorithm

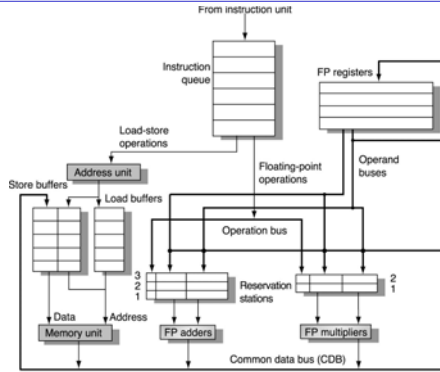
DIV.D F0, F2, F4  
 ADD.D S, F0, F8  
 S.D S, 0(R1) → register renaming  
 SUB.D T, F10, F14  
 MUL.D F6, F10, T

- Implemented through reservation stations (rs) per functional unit
  - Buffers an operand as soon as it is available – avoids WAR hazards.
  - Pending instr. designate rs that will provide their inputs – avoids WAW hazards.
  - The last write in a sequence of same-register-writing actually updates the register
  - Decentralize hazard detection and execution control
  - Instruction results are passed directly to the FU from rs rather than from registers
    - ❖ Through common data bus (CDB)

## Another Dynamic Algorithm: Tomasulo Algorithm

- For IBM 360/91 about 3 years after CDC 6600
- Goal: High Performance without special compilers
- Differences between Tomasulo Algorithm & Scoreboard
  - Control & buffers distributed with Function Units vs. centralized in scoreboard; called "reservation stations"
  - Registers in instructions replaced by pointers to reservation station buffer
  - HW renaming of registers to avoid WAW hazards
  - Buffer operand values to avoid WAR hazards
  - Common Data Bus broadcasts results to all FUs
  - Load and Stores treated as FUs as well
- Why study? Lead to Alpha 21264, HP 8000, MIPS 10000, Pentium II, Power PC 604 ...

## FP unit and load-store unit using Tomasulo's alg.



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## Reservation Station Components

$Op$ —Operation to perform in the unit (e.g., + or -)

$V_j, V_k$ —Value of Source operands

- store buffers have  $V$  field, the value to be stored

$Q_j, Q_k$ —Reservation stations producing source registers

- No ready flags as in Scoreboard;  $Q_j, Q_k=0 \Rightarrow$  ready

Busy—Indicates reservation station or FU is busy

Register result status—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions that will write that register.

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## Three Stages of Tomasulo Algorithm

### 1. Issue—get instruction from FP Op Queue

Check for structure hazards. If reservation station ( $r$ ) is free, the issue logic issues instr to  $r$  & read operands into  $r$  if they are ready. Perform register renaming – put  $r$  into the register status table for the destination register.

### 2. Execution—operate on operands (EX)

When both operands are ready then execute; if not ready, watch CDB for result

### 3. Write result—finish execution (WB)

Write on Common Data Bus to all awaiting units; mark reservation station available. Write result into dest. reg. if its status is  $r$ .

- Normal data bus: data + destination ("go to" bus)
- CDB: data + source ("come from" bus)
  - 64 bits of data + 4 bits of Functional Unit source address
  - Write if matches expected Functional Unit (produces result)
  - Does broadcast

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## Tomasulo Example Cycle 0

Instruction status				Execution		Write						
Instruction	$j$	$k$	Issue	complete	Result			Busy	Address			
LD	F6	34+	R2					Load1	No			
LD	F2	45+	R3					Load2	No			
MULTD	F0	F2	F4					Load3	No			
SUBD	F8	F6	F2									
DIVD	F10	F0	F6									
ADDD	F6	F8	F2									
Reservation Stations				S1	S2	RS for j RS for k						
Time	Name	Busy	Op	$V_j$	$V_k$	$Q_j$	$Q_k$					
0	Add1	No										
0	Add2	No										
	Add3	No										
0	Mult1	No										
0	Mult2	No										
Register result status												
Clock			FU	F0	F2	F4	F6	F8	F10	F12	...	F30
0			FU									

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### Tomasulo Example Cycle 1

Instruction status				Execution	Write													
Instruction	j	k	Issue	complete	Result			Busy	Address									
LD	F6	34+	R2	1				Load1	Yes	34+R2								
LD	F2	45+	R3					Load2	No									
MULTD	F0	F2	F4					Load3	No									
SUBD	F8	F6	F2															
DIVD	F10	F0	F6															
ADD	F6	F8	F2															
Reservation Stations				S1	S2	RS for j	RS for k											
Time Name	Busy	Op	Vj	Vk	Qj	Qk												
0 Add1	No																	
0 Add2	No																	
0 Add3	No																	
0 Mult1	No																	
0 Mult2	No																	
Register result status																		
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30								
1		FU			Load1													

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### Tomasulo Example Cycle 2

Instruction status				Execution	Write													
Instruction	j	k	Issue	complete	Result			Busy	Address									
LD	F6	34+	R2	1	2-			Load1	Yes	34+R2								
LD	F2	45+	R3	2				Load2	Yes	45+R3								
MULTD	F0	F2	F4					Load3	No									
SUBD	F8	F6	F2															
DIVD	F10	F0	F6															
ADD	F6	F8	F2															
Reservation Stations				S1	S2	RS for j	RS for k											
Time Name	Busy	Op	Vj	Vk	Qj	Qk												
0 Add1	No																	
0 Add2	No																	
0 Add3	No																	
0 Mult1	No																	
0 Mult2	No																	
Register result status																		
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30								
2		FU	Load2		Load1													

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### Tomasulo Example Cycle 3

Instruction status				Execution	Write													
Instruction	j	k	Issue	complete	Result			Busy	Address									
LD	F6	34+	R2	1	2-3			Load1	Yes	34+R2								
LD	F2	45+	R3	2	3-			Load2	Yes	45+R3								
MULTD	F0	F2	F4	3				Load3	No									
SUBD	F8	F6	F2															
DIVD	F10	F0	F6															
ADD	F6	F8	F2															
Reservation Stations				S1	S2	RS for j	RS for k											
Time Name	Busy	Op	Vj	Vk	Qj	Qk												
0 Add1	No																	
0 Add2	No																	
0 Add3	No																	
0 Mult1	Yes	Mult																
0 Mult2	No																	
Register result status																		
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30								
3		FU	Mult1	Load2	Load1													

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### Tomasulo Example Cycle 4

Instruction status				Execution	Write													
Instruction	j	k	Issue	complete	Result			Busy	Address									
LD	F6	34+	R2	1	2-3	4		Load1	No									
LD	F2	45+	R3	2	3-4			Load2	Yes	45+R3								
MULTD	F0	F2	F4	3				Load3	No									
SUBD	F8	F6	F2	4														
DIVD	F10	F0	F6															
ADD	F6	F8	F2															
Reservation Stations				S1	S2	RS for j	RS for k											
Time Name	Busy	Op	Vj	Vk	Qj	Qk												
0 Add1	Yes	Sub	M(A1)															
0 Add2	No																	
0 Add3	No																	
0 Mult1	Yes	Mult																
0 Mult2	No																	
Register result status																		
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30								
4		FU	Mult1	Load2	M(A1)	Add1												

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### Tomasulo Example Cycle 5

Instruction status				Execution	Write								
Instruction	j	k	Issue	complete	Result			Busy	Address				
LD	F6	34+	R2	1	2-3	4		Load1	No				
LD	F2	45+	R3	2	3-4	5		Load2	No				
MULTD	F0	F2	F4	3				Load3	No				
SUBD	F8	F6	F2	4									
DIVD	F10	F0	F6	5									
ADD	F6	F8	F2										
Reservation Stations				S1	S2	RS for j	RS for k						
Time Name	Busy	Op	Vj	Vk	Qj	Qk							
2	Add1	Yes	Sub	M(A1)	M(A2)								
0	Add2	No											
	Add3	No											
10	Mult1	Yes	Mult	M(A2)	R(F4)								
0	Mult2	Yes	Div		M(A1)	Mult1							
Register result status													
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30		
5			FU	Mult1	M(A2)		M(A1)	Add1	Mult2				

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### Tomasulo Example Cycle 6

Instruction status				Execution	Write								
Instruction	j	k	Issue	complete	Result			Busy	Address				
LD	F6	34+	R2	1	2-3	4		Load1	No				
LD	F2	45+	R3	2	3-4	5		Load2	No				
MULTD	F0	F2	F4	3	6 --			Load3	No				
SUBD	F8	F6	F2	4	6 --								
DIVD	F10	F0	F6	5									
ADD	F6	F8	F2	6									
Reservation Stations				S1	S2	RS for j	RS for k						
Time Name	Busy	Op	Vj	Vk	Qj	Qk							
1	Add1	Yes	Sub	M(A1)	M(A2)								
0	Add2	Yes	Add		M(A2)	Add1							
	Add3	No											
9	Mult1	Yes	Mult	M(A2)	R(F4)								
0	Mult2	Yes	Div		M(A1)	Mult1							
Register result status													
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30		
6			FU	Mult1	M(A2)		M(A1)	Add2	Add1	Mult2			

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### Tomasulo Example Cycle 7

Instruction status				Execution	Write								
Instruction	j	k	Issue	complete	Result			Busy	Address				
LD	F6	34+	R2	1	2-3	4		Load1	No				
LD	F2	45+	R3	2	3-4	5		Load2	No				
MULTD	F0	F2	F4	3	6 --			Load3	No				
SUBD	F8	F6	F2	4	6 --								
DIVD	F10	F0	F6	5									
ADD	F6	F8	F2	6									
Reservation Stations				S1	S2	RS for j	RS for k						
Time Name	Busy	Op	Vj	Vk	Qj	Qk							
0	Add1	Yes	Sub	M(A1)	M(A2)								
0	Add2	Yes	Add		M(A2)	Add1							
	Add3	No											
8	Mult1	Yes	Mult	M(A2)	R(F4)								
0	Mult2	Yes	Div		M(A1)	Mult1							
Register result status													
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30		
7			FU	Mult1	M(A2)		Add2	Add1	Mult2				

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### Tomasulo Example Cycle 8

Instruction status				Execution	Write								
Instruction	j	k	Issue	complete	Result			Busy	Address				
LD	F6	34+	R2	1	2-3	4		Load1	No				
LD	F2	45+	R3	2	3-4	5		Load2	No				
MULTD	F0	F2	F4	3	6 --			Load3	No				
SUBD	F8	F6	F2	4	6 --	0							
DIVD	F10	F0	F6	5									
ADD	F6	F8	F2	6									
Reservation Stations				S1	S2	RS for j	RS for k						
Time Name	Busy	Op	Vj	Vk	Qj	Qk							
0	Add1	No											
2	Add2	Yes	Add	M1-M2	M(A2)								
	Add3	No											
7	Mult1	Yes	Mult	M(A2)	R(F4)								
0	Mult2	Yes	Div		M(A1)	Mult1							
Register result status													
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30		
8			FU	Mult1	M(A2)		Add2	M1-M2	Mult2				

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## Tomasulo Example Cycle 9

Instruction status				Execution	Write				Busy	Address
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6--			Load3	No	
SUBD	F8	F6	F2	4	6--7	8				
DIVD	F10	F0	F6	5						
ADDD	F6	F8	F2	6	9--					
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
1 Add2	Yes	Add	M1-M2	M(A2)						
Add3	No									
6 Mult1	Yes	Mult	M(A2)	R(F4)						
0 Mult2	Yes	Div		M(A1)	Mult1					
Register result status										
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
9		FU	Mult1	M(A2)	Add2	M1-M2	Mult2			

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## Tomasulo Example Cycle 10

Instruction status				Execution	Write				Busy	Address
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6--			Load3	No	
SUBD	F8	F6	F2	4	6--7	8				
DIVD	F10	F0	F6	5						
ADDD	F6	F8	F2	6	9--10					
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
0 Add2	Yes	Add	M1-M2	M(A2)						
Add3	No									
5 Mult1	Yes	Mult	M(A2)	R(F4)						
0 Mult2	Yes	Div		M(A1)	Mult1					
Register result status										
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
10		FU	Mult1	M(A2)	Add2	M1-M2	Mult2			

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## Tomasulo Example Cycle 11

Instruction status				Execution	Write				Busy	Address
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6--			Load3	No	
SUBD	F8	F6	F2	4	6--7	8				
DIVD	F10	F0	F6	5						
ADDD	F6	F8	F2	6	9--10	11				
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
Add2	No									
Add3	No									
4 Mult1	Yes	Mult	M(A2)	R(F4)						
0 Mult2	Yes	Div		M(A1)	Mult1					
Register result status										
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
11		FU	Mult1	M(A2)	M1-M2+M(A1)	M1-M2	Mult2			

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## Tomasulo Example Cycle 12

Instruction status				Execution	Write				Busy	Address
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6--			Load3	No	
SUBD	F8	F6	F2	4	6--7	8				
DIVD	F10	F0	F6	5						
ADDD	F6	F8	F2	6	9--10	11				
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
Add2	No									
Add3	No									
4 Mult1	Yes	Mult	M(A2)	R(F4)						
0 Mult2	Yes	Div		M(A1)	Mult1					
Register result status										
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
12		FU	Mult1	M(A2)	M1-M2+M(A1)	M1-M2	Mult2			

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## Tomasulo Example Cycle 15

Instruction status				Execution	Write			Busy	Address	
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6-15			Load3	No	
SUBD	F8	F6	F2	4	6-7	8				
DIVD	F10	F0	F6	5						
ADDD	F6	F8	F2	6	9-10	11				
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
Add2	No									
Add3	No									
0 Mult1	Yes	Mult	M(A2)	R(F4)						
0 Mult2	Yes	Div		M(A1)	Mult1					
Register result status										
Clock	F0	F2	F4	F6	F8	F10	F12	...	F30	
15	FU	M(A2)		M1-M2+M(A1)	M1-M2	Mult2				

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## Tomasulo Example Cycle 16

Instruction status				Execution	Write			Busy	Address	
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6-15	16		Load3	No	
SUBD	F8	F6	F2	4	6-7	8				
DIVD	F10	F0	F6	5						
ADDD	F6	F8	F2	6	9-10	11				
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
Add2	No									
Add3	No									
0 Mult1	No									
40 Mult2	Yes	Div	M*F4	M(A1)						
Register result status										
Clock	F0	F2	F4	F6	F8	F10	F12	...	F30	
16	FU	M*F4	M(A2)	M1-M2+M(A1)	M1-M2	Mult2				

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## Tomasulo Example Cycle 56

Instruction status				Execution	Write			Busy	Address	
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6-15	16		Load3	No	
SUBD	F8	F6	F2	4	6-7	8				
DIVD	F10	F0	F6	5	17-56					
ADDD	F6	F8	F2	6	9-10	11				
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
Add2	No									
Add3	No									
0 Mult1	No									
0 Mult2	Yes	Div	M*F4	M(A1)						
Register result status										
Clock	F0	F2	F4	F6	F8	F10	F12	...	F30	
56	FU	M*F4	M(A2)	M1-M2+M(A1)	M1-M2	Mult2				

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## Tomasulo Example Cycle 57

Instruction status				Execution	Write			Busy	Address	
Instruction	j	k	Issue	complete	Result					
LD	F6	34+	R2	1	2-3	4		Load1	No	
LD	F2	45+	R3	2	3-4	5		Load2	No	
MULTD	F0	F2	F4	3	6-15	16		Load3	No	
SUBD	F8	F6	F2	4	6-7	8				
DIVD	F10	F0	F6	5	17-56	57				
ADDD	F6	F8	F2	6	9-10	11				
Reservation Stations				S1	S2	RS for j RS for k				
Time Name	Busy	Op	Vj	Vk	Qj	Qk				
0 Add1	No									
Add2	No									
Add3	No									
0 Mult1	No									
0 Mult2	No									
Register result status										
Clock	F0	F2	F4	F6	F8	F10	F12	...	F30	
57	FU	M*F4	M(A2)	M1-M2+M(A1)	M1-M2	result				

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## Tomasulo Loop Example

```

Loop: LD      F0  0  R1
      MULTD   F4  F0 F2
      SD      F4  0  R1
      SUBI    R1  R1  #8
      BNEZ   R1  Loop
    
```

- Multiply takes 4 clocks
- First load takes 8 clocks (cache misses), second load takes 1 clock (hit)
- To be clear, will show clocks for SUBI, BNEZ (integer instr.)
- Reality: integer instructions are ahead

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## Loop Example Cycle 0

Instruction status				Execution/Write					
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0	R1	1			Load1	No	
MULTD	F4	F0	F2	1			Load2	No	
SD	F4	0	R1	1			Load3	Qi V	
LD	F0	0	R1	2			Store1	No	
MULTD	F4	F0	F2	2			Store2	No	
SD	F4	0	R1	2			Store3	No	

Reservation Stations			S1	S2	RS for j, RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:
0	Add1	No						LD F0 0 R1
0	Add2	No						MULT F4 F0 F2
0	Add3	No						SD F4 0 R1
0	Mult1	No						SUBI R1 R1 #8
0	Mult2	No						BNEZ R1 Loop

Register result status												
Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30		
No 2, 2004	80	Qi										26

## Loop Example Cycle 1

Instruction status				Execution/Write					
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0	R1	1	1		Load1	Yes 80	
MULTD	F4	F0	F2	1			Load2	No	
SD	F4	0	R1	1			Load3	No Qi V	
LD	F0	0	R1	2			Store1	No	
MULTD	F4	F0	F2	2			Store2	No	
SD	F4	0	R1	2			Store3	No	

Reservation Stations			S1	S2	RS for j, RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:
0	Add1	No						LD F0 0 R1
0	Add2	No						MULT F4 F0 F2
0	Add3	No						SD F4 0 R1
0	Mult1	No						SUBI R1 R1 #8
0	Mult2	No						BNEZ R1 Loop

Register result status												
Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30		
No 2, 2004	80	Qi	Load1									27

## Loop Example Cycle 2

Instruction status				Execution/Write					
Instruction	j	k	iteration	Issue	complete	Result	Busy	Address	
LD	F0	0	R1	1	1	2	Load1	Yes 80	
MULTD	F4	F0	F2	1	2		Load2	No	
SD	F4	0	R1	1			Load3	No Qi V	
LD	F0	0	R1	2			Store1	No	
MULTD	F4	F0	F2	2			Store2	No	
SD	F4	0	R1	2			Store3	No	

Reservation Stations			S1	S2	RS for j, RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:
0	Add1	No						LD F0 0 R1
0	Add2	No						MULT F4 F0 F2
0	Add3	No						SD F4 0 R1
0	Mult1	Yes	Mult			R(F2)	Load1	SUBI R1 R1 #8
0	Mult2	No						BNEZ R1 Loop

Register result status												
Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30		
No 2, 2004	80	Qi	Load1	L	Mult1							28

### Loop Example Cycle 3

Instruction status				Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Address				
LD	F0	0	R1	1	1	2--	Load1	Yes 80				
MULTD	F4	F0	F2	1	2		Load2	No				
SD	F4	0	R1	1	3		Load3	No Q V				
LD	F0	0	R1	2			Store1	Yes 80 Mult1				
MULTD	F4	F0	F2	2			Store2	No				
SD	F4	0	R1	2			Store3	No				
Reservation Stations				S1	S2	RS for	RS for	k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:				
0	Add1	No						LD F0 0 R1				
0	Add2	No						MULT F4 F0 F2				
0	Add3	No						SD F4 0 R1				
0	Mult1	Yes	Mult		R(F2)	Load1		SUBI R1 R1 #8				
0	Mult2	No						BNEZ R1 Loop				
Register result status				F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	Nov. 2, 2004	R1	Qi	Load1	Mult1	7						29

### Loop Example Cycle 4

Instruction status				Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Address				
LD	F0	0	R1	1	1	2--	Load1	Yes 80				
MULTD	F4	F0	F2	1	2		Load2	No				
SD	F4	0	R1	1	3		Load3	No Q V				
LD	F0	0	R1	2			Store1	Yes 80 Mult1				
MULTD	F4	F0	F2	2			Store2	No				
SD	F4	0	R1	2			Store3	No				
Reservation Stations				S1	S2	RS for	RS for	k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:				
0	Add1	No						LD F0 0 R1				
0	Add2	No						MULT F4 F0 F2				
0	Add3	No						SD F4 0 R1				
0	Mult1	Yes	Mult		R(F2)	Load1		SUBI R1 R1 #8				
0	Mult2	No						BNEZ R1 Loop				
Register result status				F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	Nov. 2, 2004	R1	Qi	Load1	Mult1	7						30

### Loop Example Cycle 5

Instruction status				Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Address				
LD	F0	0	R1	1	1	2--	Load1	Yes 80				
MULTD	F4	F0	F2	1	2		Load2	No				
SD	F4	0	R1	1	3		Load3	No Q V				
LD	F0	0	R1	2			Store1	Yes 80 Mult1				
MULTD	F4	F0	F2	2			Store2	No				
SD	F4	0	R1	2			Store3	No				
Reservation Stations				S1	S2	RS for	RS for	k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:				
0	Add1	No						LD F0 0 R1				
0	Add2	No						MULT F4 F0 F2				
0	Add3	No						SD F4 0 R1				
0	Mult1	Yes	Mult		R(F2)	Load1		SUBI R1 R1 #8				
0	Mult2	No						BNEZ R1 Loop				
Register result status				F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	Nov. 2, 2004	R1	Qi	Load1	Mult1	7						31

### Loop Example Cycle 6: F0 never sees load from location 80

Instruction status				Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Address				
LD	F0	0	R1	1	1	2--	Load1	Yes 80				
MULTD	F4	F0	F2	1	2		Load2	Yes 72				
SD	F4	0	R1	1	3		Load3	No Q V				
LD	F0	0	R1	2		6	Store1	Yes 80 Mult1				
MULTD	F4	F0	F2	2			Store2	No				
SD	F4	0	R1	2			Store3	No				
Reservation Stations				S1	S2	RS for	RS for	k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:				
0	Add1	No						LD F0 0 R1				
0	Add2	No						MULT F4 F0 F2				
0	Add3	No						SD F4 0 R1				
0	Mult1	Yes	Mult		R(F2)	Load1		SUBI R1 R1 #8				
0	Mult2	No						BNEZ R1 Loop				
Register result status				F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	Nov. 2, 2004	R1	Qi	Load2	Mult1	7						32

### Loop Example Cycle 7: Register file completely detached from iteration 1

Instruction status				Execution/Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Load1	Load2	
LD	F0	0	R1	1	1	2--	Yes	80	
MULTD	F4	F0	F2	1	2		Yes	72	
SD	F4	0	R1	1	3		No	Q V	
LD	F0	0	R1	2	6		Yes	80 Mult1	
MULTD	F4	F0	F2	2	7		No		
SD	F4	0	R1	2			No		

Reservation Stations		S1	S2	RS for		RS for k	
Time	Name	Busy	Op	Vj	Vk	Qj	Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	Yes	Mult		R(F2)	Load1	
0	Mult2	Yes	Mult		R(F2)	Load2	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1									
7	Nov. 2, 2004	72	Qi	Load2	Mult2					33

### Loop Example Cycle 8: First and second iteration completely overlapped

Instruction status				Execution/Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Load1	Load2	
LD	F0	0	R1	1	1	2--	Yes	80	
MULTD	F4	F0	F2	1	2		Yes	72	
SD	F4	0	R1	1	3		No	Q V	
LD	F0	0	R1	2	6		Yes	80 Mult1	
MULTD	F4	F0	F2	2	7		Yes	72 Mult2	
SD	F4	0	R1	2	8		No		

Reservation Stations		S1	S2	RS for		RS for k	
Time	Name	Busy	Op	Vj	Vk	Qj	Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	Yes	Mult		R(F2)	Load1	
0	Mult2	Yes	Mult		R(F2)	Load2	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1									
8	Nov. 2, 2004	72	Qi	Load2	Mult2					34

### Loop Example Cycle 9

Instruction status				Execution/Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Load1	Load2	
LD	F0	0	R1	1	1	2--9	Yes	80	
MULTD	F4	F0	F2	1	2		Yes	72	
SD	F4	0	R1	1	3		No	Q V	
LD	F0	0	R1	2	6		Yes	80 Mult1	
MULTD	F4	F0	F2	2	7		Yes	72 Mult2	
SD	F4	0	R1	2	8		No		

Reservation Stations		S1	S2	RS for		RS for k	
Time	Name	Busy	Op	Vj	Vk	Qj	Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	Yes	Mult		R(F2)	Load1	
0	Mult2	Yes	Mult		R(F2)	Load2	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1									
9	Nov. 2, 2004	72	Qi	Load2	Mult2					33

### Loop Example Cycle 10

Instruction status				Execution/Write				Busy Address	
Instruction	j	k	iteration	Issue	complete	Result	Load1	Load2	
LD	F0	0	R1	1	1	2--9	No		
MULTD	F4	F0	F2	1	2		Yes	72	
SD	F4	0	R1	1	3		No	Q V	
LD	F0	0	R1	2	6	10	Yes	80 Mult1	
MULTD	F4	F0	F2	2	7		Yes	72 Mult2	
SD	F4	0	R1	2	8		No		

Reservation Stations		S1	S2	RS for		RS for k	
Time	Name	Busy	Op	Vj	Vk	Qj	Qk
0	Add1	No					
0	Add2	No					
0	Add3	No					
4	Mult1	Yes	Mult		M[80]	R(F2)	
0	Mult2	Yes	Mult		R(F2)	Load2	

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1									
10	Nov. 2, 2004	64	Qi	Load2	Mult2					34

### Loop Example Cycle 11

Instruction status			Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Store			
LD	F0	0	R1	1	1	2--9	10	Load1	No		
MULTD	F4	F0	F2	1	2			Load2	No		
SD	F4	0	R1	1	3			Load3	Yes 64		
LD	F0	0	R1	2	6	10	11	Store1	Yes 80 Mult1		
MULTD	F4	F0	F2	2	7			Store2	Yes 72 Mult2		
SD	F4	0	R1	2	8			Store3	No		
Reservation Stations			S1	S2	RS for		RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD F0 0 R1			
0	Add2	No						MULT F4 F0 F2			
0	Add3	No						SD F4 0 R1			
3	Mult1	Yes	Mult	M[80]	R(F2)			SUBI R1 R1 #8			
4	Mult2	Yes	Mult	M[72]	R(F2)			BNEZ R1 Loop			
Register result status			F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1										
11 <sup>Nov</sup>	2, 2004	64	Qi	Load3	Mult2 <sup>7</sup>						31

### Loop Example Cycle 12: Why not issue 3<sup>rd</sup> multiply

Instruction status			Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Store			
LD	F0	0	R1	1	1	2--9	10	Load1	No		
MULTD	F4	F0	F2	1	2			Load2	No		
SD	F4	0	R1	1	3			Load3	Yes 64		
LD	F0	0	R1	2	6	10	11	Store1	Yes 80 Mult1		
MULTD	F4	F0	F2	2	7			Store2	Yes 72 Mult2		
SD	F4	0	R1	2	8			Store3	No		
Reservation Stations			S1	S2	RS for		RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD F0 0 R1			
0	Add2	No						MULT F4 F0 F2			
0	Add3	No						SD F4 0 R1			
2	Mult1	Yes	Mult	M[80]	R(F2)			SUBI R1 R1 #8			
3	Mult2	Yes	Mult	M[72]	R(F2)			BNEZ R1 Loop			
Register result status			F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1										
12 <sup>Nov</sup>	2, 2004	64	Qi	Load3	Mult2 <sup>7</sup>						38

### Loop Example Cycle 14

Instruction status			Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Store			
LD	F0	0	R1	1	1	2--9	10	Load1	No		
MULTD	F4	F0	F2	1	2	14		Load2	No		
SD	F4	0	R1	1	3			Load3	Yes 64		
LD	F0	0	R1	2	6	10	11	Store1	Yes 80 Mult1		
MULTD	F4	F0	F2	2	7			Store2	Yes 72 Mult2		
SD	F4	0	R1	2	8			Store3	No		
Reservation Stations			S1	S2	RS for		RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD F0 0 R1			
0	Add2	No						MULT F4 F0 F2			
0	Add3	No						SD F4 0 R1			
0	Mult1	Yes	Mult	M[80]	R(F2)			SUBI R1 R1 #8			
1	Mult2	Yes	Mult	M[72]	R(F2)			BNEZ R1 Loop			
Register result status			F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1										
14 <sup>Nov</sup>	2, 2004	64	Qi	Load3	Mult2 <sup>7</sup>						34

### Loop Example Cycle 15

Instruction status			Execution/Write				Busy Address				
Instruction	j	k	iteration	Issue	complete	Result	Load	Store			
LD	F0	0	R1	1	1	2--9	10	Load1	No		
MULTD	F4	F0	F2	1	2	14	15	Load2	No		
SD	F4	0	R1	1	3			Load3	Yes 64		
LD	F0	0	R1	2	6	10	11	Store1	Yes 80 Mult1		
MULTD	F4	F0	F2	2	7	15		Store2	Yes 72 Mult2		
SD	F4	0	R1	2	8			Store3	No		
Reservation Stations			S1	S2	RS for		RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD F0 0 R1			
0	Add2	No						MULT F4 F0 F2			
0	Add3	No						SD F4 0 R1			
0	Mult1	No						SUBI R1 R1 #8			
0	Mult2	Yes	Mult	M[72]	R(F2)			BNEZ R1 Loop			
Register result status			F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	R1										
15 <sup>Nov</sup>	2, 2004	64	Qi	Load3	Mult2 <sup>7</sup>						44

## Loop Example Cycle 16 ...

Instruction status				Execution/Write			Busy Address		
Instruction	j	k	iteration	Issue	complete	Result	Load1	Load2	Load3
LD	F0	0	R1	1	2--9	10	No		
MULTD	F4	F0	F2	1	2	14	15	No	
SD	F4	0	R1	1	3			Yes	64 Q V
LD	F0	0	R1	2	6	10	11	Yes	80 80*R2
MULTD	F4	F0	F2	2	7	15	16	Yes	72 Mult2 70*R2
SD	F4	0	R1	2	8			No	
Reservation Stations				S1	S2	RS for	RS for k		
Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:	
0	Add1	No						LD	F0 0 R1
0	Add2	No						MULT	F4 F0 F2
0	Add3	No						SD	F4 0 R1
0	Mult1	No						SUBI	R1 R1 #8
0	Mult2	No						BNEZ	R1 Loop
Register result status									
Clock		R1		F0	F2	F4	F6	F8	F10 F12 ... F30
16	Nov. 2, 2004	64	Q1	Load3		Mult37			4

## Tomasulo Summary

- Prevents Register as bottleneck
- Avoids WAR, WAW hazards of Scoreboard
- Allows loop unrolling in HW
- Not limited to basic blocks (provided branch prediction)
- Lasting Contributions
  - Dynamic scheduling
  - Register renaming
  - Load/store disambiguation (Read Pg. 195 in your textbook!)