

Lecture 6

Overcoming Pipeline Hazards:  
Dynamic Scheduling via  
Scoreboarding

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HW Schemes: Instruction Parallelism

- *Compiler or Static* instruction scheduling can avoid some pipeline hazards.
  - e.g. filling branch delay slot.
- **Why in HW at run time?**
  - Works when can't know dependence at compile time
    - ✦ WAW can only be detected at run time
  - Compiler simpler
  - Code for one machine runs well on another
- **Key idea: Allow instructions behind stall to proceed**

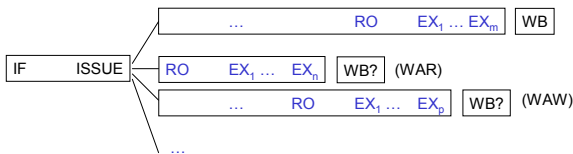
```

DIVD    F0, F2, F4
ADD    F10, F0, F8
SUBD   F8, F8, F14
            
```

  - Enables out-of-order execution => out-of-order completion
  - But, both structural and data hazards are checked in MIPS
    - ✦ ADDD is stalled at ID, SUBD can not even proceed to ID.

HW Schemes: Instruction Parallelism

- **Out-of-order execution divides ID stage:**
  1. **Issue**—decode instructions, check for structural hazards
  2. **Read operands (RO)**—wait until no data hazards, then read operands
    - > ADDD would stall at RO, and SUBD could proceed with no stalls.
- **Scoreboards allow instruction to execute whenever 1 & 2 hold, not waiting for prior instructions.**



Focusing on FP operations - assume no MEM stages

Scoreboard Implications

- **Out-of-order completion => WAR, WAW hazards**
- **Solutions for WAR**
  - CDC 6600: Stall Write to allow Reads to take place; Read registers only during Read Operands stage.
  - Tomasulo: Queue both the operation and copies of its operands
- **For WAW, must detect hazard: stall until other completes**
- **Need to have multiple instructions in execution phase => multiple execution units or pipelined execution units**
- **Scoreboard replaces ID, EX, WB with 4 stages**
- **Scoreboard keeps track of dependencies, state or operations**
  - Monitors every change in the hardware.
  - Determines when to read ops, when can execute, when can wb.
  - Hazard detection and resolution is centralized.

## Four Stages of Scoreboard Control

### 1. Issue—decode instructions & check for structural hazards (ID1)

If a functional unit for the instruction is free and no other active instruction has the same destination register (WAW), the scoreboard issues the instruction to the functional unit and updates its internal data structure. If a structural or WAW hazard exists, then the instruction issue stalls, and no further instructions will issue until these hazards are cleared.

### 2. Read operands—wait until no data hazards, then read operands (ID2)

A source operand is available if no earlier issued active instruction is going to write it, or if the register containing the operand is being written by a currently active functional unit. When the source operands are available, the scoreboard tells the functional unit to proceed to read the operands from the registers and begin execution. The scoreboard resolves RAW hazards dynamically in this step, and instructions may be sent into execution out of order.

Oct. 26, 2004

5

## Four Stages of Scoreboard Control

### 3. Execution—operate on operands (EX)

The functional unit begins execution upon receiving operands. When the result is ready, it notifies the scoreboard that it has completed execution.

### 4. Write result—finish execution (WB)

Once the scoreboard is aware that the functional unit has completed execution, the scoreboard checks for WAR hazards. If none, it writes results. If WAR, then it stalls the instruction.

Example:

```

DIVD  F0,F2,F4
ADDD  F10,F0,F8
SUBD  F8,F8,F14
    
```

CDC 6600 scoreboard would stall SUBD until ADDD reads operands

Oct. 26, 2004

6

## Three Parts of the Scoreboard

### 1. Instruction status—which of 4 steps the instruction is in

### 2. Functional unit status—Indicates the state of the functional unit (FU). 9 fields for each functional unit

**Busy**—Indicates whether the unit is busy or not

**Op**—Operation to perform in the unit (e.g., + or -)

**Fi**—Destination register

**Fj, Fk**—Source-register numbers

**Qj, Qk**—Functional units producing source registers Fj, Fk

**Rj, Rk**—Flags indicating when Fj, Fk are ready

### 3. Register result status—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions will write that register

Oct. 26, 2004

7

## Detailed Scoreboard Pipeline Control

Instruction status	Wait until	Bookkeeping
<b>Issue</b>	Not busy (FU) and not result(D)	Busy(FU)← yes; Op(FU)← op; Fi(FU)← `D'; Fj(FU)← `S1'; Fk(FU)← `S2'; Qj← Result(`S1'); Qk← Result(`S2'); Rj← not Qj; Rk← not Qk; Result(`D')← FU;
<b>Read operands</b>	Rj and Rk	Rj← No; Rk← No
<b>Execution complete</b>	Functional unit done	
<b>Write result</b>	$\forall f((Fj(f)) \neq Fi(FU) \text{ or } Rj(f) = \text{No}) \& (Fk(f)) \neq Fi(FU) \text{ or } Rk(f) = \text{No})$	$\forall f(\text{if } Qj(f) = \text{FU then } Rj(f) \leftarrow \text{Yes}; \forall f(\text{if } Qk(f) = \text{FU then } Rj(f) \leftarrow \text{Yes}); \text{Result}(Fi(FU)) \leftarrow 0; \text{Busy}(FU) \leftarrow \text{No}$

WAW

WAR

A.55 on page A-76

Oct. 26, 2004

8

## Scoreboard Example

- The following numbers are to illustrate behavior, not representative
- LD - 1 cycle
  - (compute address + data cache access)
- ADDDs and SUBs are 2 cycles
- Multiply is 10 cycles
- Divide is 40 cycles

Oct. 26, 2004

9

## Scoreboard Example

Instruction status			Read		Execution		Write	
Instruction	j	k	Issue	operand complete	Result			
LD	F6	34+ R2						
LD	F2	45+ R3						
MULT	F0	F2 F4						
SUBD	F8	F6 F2						
DIVD	F10	F0 F6						
ADDD	F6	F8 F2						

Functional unit status		dest		S1	S2	FU for j		FU for k		Fk?
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer		No								
Mult1		No								
Mult2		No								
Add		No								
Divide		No								

Register result status												
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30		
1	FU	Integer										

Oct. 26, 2004

10

## Scoreboard Example Cycle 1

Instruction status			Read		Execution		Write	
Instruction	j	k	Issue	operand complete	Result			
LD	F6	34+ R2	1					
LD	F2	45+ R3						
MULT	F0	F2 F4						
SUBD	F8	F6 F2						
DIVD	F10	F0 F6						
ADDD	F6	F8 F2						

Functional unit status		dest		S1	S2	FU for j		FU for k		Fk?
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer		Yes	Load	F6		R2				Yes
Mult1		No								
Mult2		No								
Add		No								
Divide		No								

Register result status												
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30		
1	FU	Integer										

Oct. 26, 2004

11

## Scoreboard Example Cycle 2

Instruction status			Read		Execution		Write	
Instruction	j	k	Issue	operand complete	Result			
LD	F6	34+ R2	1	2				
LD	F2	45+ R3						
MULT	F0	F2 F4						
SUBD	F8	F6 F2						
DIVD	F10	F0 F6						
ADDD	F6	F8 F2						

Functional unit status		dest		S1	S2	FU for j		FU for k		Fk?
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer		Yes	Load	F6		R2				No
Mult1		No								
Mult2		No								
Add		No								
Divide		No								

Register result status												
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30		
2	FU	Integer										

Oct. 26, 2004

12

### Scoreboard Example Cycle 3

Instruction status				Read Execution Write			
Instruction	j	k	Issue	operat	complete	Result	
LD	F6	34+	R2	1	2	3	
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADD	F6	F8	F2				

Functional unit status		dest	S1	S2	FU for	FU for	Fk?
Tim Name	Busy	Op	Fi	Fj	Fk	Qj	Qk
Integer	Yes	Load	F6		R2		No
Mult1	No						
Mult2	No						
Add	No						
Divide	No						

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	3	FU Integer									

Oct. 26, 2004

13

### Scoreboard Example Cycle 4

Instruction status				Read Execution Write			
Instruction	j	k	Issue	operat	complete	Result	
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADD	F6	F8	F2				

Functional unit status		dest	S1	S2	FU for	FU for	Fk?
Tim Name	Busy	Op	Fi	Fj	Fk	Qj	Qk
Integer	Yes	Load	F6		R2		No
Mult1	No						
Mult2	No						
Add	No						
Divide	No						

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	4	FU Integer									

Oct. 26, 2004

14

### Scoreboard Example Cycle 5

Instruction status				Read Execution Write			
Instruction	j	k	Issue	operat	complete	Result	
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3	5			
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADD	F6	F8	F2				

Functional unit status		dest	S1	S2	FU for	FU for	Fk?
Tim Name	Busy	Op	Fi	Fj	Fk	Qj	Qk
Integer	Yes	Load	F2		R3		Yes
Mult1	No						
Mult2	No						
Add	No						
Divide	No						

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	5	FU Integer									

Oct. 26, 2004

15

### Scoreboard Example Cycle 6

Instruction status				Read Execution Write			
Instruction	j	k	Issue	operat	complete	Result	
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3	5	6		
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADD	F6	F8	F2				

Functional unit status		dest	S1	S2	FU for	FU for	Fk?
Tim Name	Busy	Op	Fi	Fj	Fk	Qj	Qk
Integer	Yes	Load	F2		R3		No
Mult1	Yes	Mult	F0		F2	F4	Integer
Mult2	No						
Add	No						
Divide	No						

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	6	FU Mult Integer									

Oct. 26, 2004

16

## Scoreboard Example Cycle 7

Instruction status			Read Execution Write			
Instruction	j	k	Issue	operat	complete	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	
MULTD	F0	F2 F4	6			
SUBD	F8	F6 F2	7			
DIVD	F10	F0 F6				
ADD	F6	F8 F2				

Functional unit status		dest		S1	S2	FU for j	FU for k	Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	
Integer	Yes	Load F2		R3					No
Mult1	Yes	Mult F0	F2	F4	Integer				No Yes
Mult2	No								
Add	Yes	Subd F8	F6	F2			Integer	Yes	No
Divide	No								

Register result status		Clock										
		F0	F2	F4	F6	F8	F10	F12	...	F30		
7	7	FU	Mult	Integer		Add						

Oct. 26, 2004

17

## Scoreboard Example Cycle 8a

Instruction status			Read Execution Write			
Instruction	j	k	Issue	operands	complete	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	
MULTD	F0	F2 F4	6			
SUBD	F8	F6 F2	7			
DIVD	F10	F0 F6				
ADD	F6	F8 F2				

Functional unit status		dest		S1	S2	FU for j	FU for k	Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	
Integer	Yes	Load F2		R3					No
Mult1	Yes	Mult F0	F2	F4	Integer				No Yes
Mult2	No								
Add	Yes	Sub F8	F6	F2			Integer	Yes	No
Divide	Yes	Div F10	F0	F6	Mult1				No Yes

Register result status		Clock										
		F0	F2	F4	F6	F8	F10	F12	...	F30		
8	8	FU	Mult1	Integer		Add	Divide					

Oct. 26, 2004

18

## Scoreboard Example Cycle 8b

Instruction status			Read EX Write			
Instruction	j	k	Issue	Op	compl.	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	8
MULTD	F0	F2 F4	6			
SUBD	F8	F6 F2	7			
DIVD	F10	F0 F6	8			
ADD	F6	F8 F2				

Functional unit status		dest		S1	S2	FU for j	FU for k	Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	
Integer	No								
Mult1	Yes	Mult F0	F2	F4					Yes Yes
Mult2	No								
Add	Yes	Sub F8	F6	F2					Yes Yes
Divide	Yes	Div F10	F0	F6	Mult1				No Yes

Register result status		Clock										
		F0	F2	F4	F6	F8	F10	F12	...	F30		
8	8	FU	Mult1		Add	Divide						19

Oct. 26, 2004

19

## Scoreboard Example Cycle 9

Instruction status			Read EX Write			
Instruction	j	k	Issue	Op	compl.	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	8
MULTD	F0	F2 F4	6	9		
SUBD	F8	F6 F2	7	9		
DIVD	F10	F0 F6	8			
ADD	F6	F8 F2				

Functional unit status		dest		S1	S2	FU for j	FU for k	Fj?	Fk?
Time Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk	
Integer	No								
10 Mult1	Yes	Mult F0	F2	F4					No No
Mult2	No								
2 Add	Yes	Sub F8	F6	F2					No No
Divide	Yes	Div F10	F0	F6	Mult1				No Yes

Register result status		Clock										
		F0	F2	F4	F6	F8	F10	F12	...	F30		
9	9	FU	Mult1		Add	Divide						

Oct. 26, 2004

20

## Scoreboard Example Cycle 11

Instruction status			Read Exec Write			
Instruction	j	k	Issue	oper	compl	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	8
MUL	F0	F2 F4	6	9		
SUB	F8	F6 F2	7	9	11	
DIV	F10	F0 F6	8			
ADD	F6	F8 F2				

Functional unit status		dest	S1	S2	FU for j	FU for k	Fj?	Fk?
TimName	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
8 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
0 Add	Yes Sub	F8	F6	F2			No	No
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	11	FU	Mult1				Add	Divide		

Oct. 26, 2004

21

## Scoreboard Example Cycle 12

Instruction status			Read Exec Write			
Instruction	j	k	Issue	oper	compl	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	8
MULTD	F0	F2 F4	6	9		
SUBD	F8	F6 F2	7	9	11	12
DIVD	F10	F0 F6	8			
ADD	F6	F8 F2				

Functional unit status		dest	S1	S2	FU for j	FU for Fj?	Fk?	
TimName	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
7 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
Add	No							
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	12	FU	Mult1				Divide			

Oct. 26, 2004

22

## Scoreboard Example Cycle 13

Instruction status			Read Exec Write			
Instruction	j	k	Issue	oper	compl	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	8
MULTD	F0	F2 F4	6	9		
SUBD	F8	F6 F2	7	9	11	12
DIVD	F10	F0 F6	8			
ADD	F6	F8 F2	13			

Functional unit status		dest	S1	S2	FU for j	FU for Fj?	Fk?	
TimName	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
6 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
Add	Yes Add	F6	F8	F2			Yes	Yes
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	13	FU	Mult1		Add	Divide				

Oct. 26, 2004

23

## Scoreboard Example Cycle 14

Instruction status			Read Exec Write			
Instruction	j	k	Issue	oper	compl	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	8
MULTD	F0	F2 F4	6	9		
SUBD	F8	F6 F2	7	9	11	12
DIVD	F10	F0 F6	8			
ADD	F6	F8 F2	13	14		

Functional unit status		dest	S1	S2	FU for j	FU for Fj?	Fk?	
TimName	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
5 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
2 Add	Yes Add	F6	F8	F2			No	No
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	14	FU	Mult1		Add	Divide				

Oct. 26, 2004

24

## Scoreboard Example Cycle 15

Instruction status			Read	Execu	Write
Instruction	j	k	Issue	operai	compl Result
LD	F6	34+ R2	1	2	3 4
LD	F2	45+ R3	5	6	7 8
MULTD	F0	F2 F4	6	9	
SUBD	F8	F6 F2	7	9	11 12
DIVD	F10	F0 F6	8		
ADD	F6	F8 F2	13	14	

Functional unit status		dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
4 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
1 Add	Yes Add	F6	F8	F2			No	No
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	15	FU									
		Mult1			Add		Divide				

Oct. 26, 2004

25

## Scoreboard Example Cycle 16

Instruction status			Read	Execu	Write
Instruction	j	k	Issue	operai	compl Result
LD	F6	34+ R2	1	2	3 4
LD	F2	45+ R3	5	6	7 8
MULTD	F0	F2 F4	6	9	
SUBD	F8	F6 F2	7	9	11 12
DIVD	F10	F0 F6	8		
ADD	F6	F8 F2	13	14	16

Functional unit status		dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
3 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
0 Add	Yes Add	F6	F8	F2			No	No
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	16	FU									
		Mult1			Add		Divide				

Oct. 26, 2004

26

## Scoreboard Example Cycle 17

Instruction status			Read	Execu	Write
Instruction	j	k	Issue	operai	compl Result
LD	F6	34+ R2	1	2	3 4
LD	F2	45+ R3	5	6	7 8
MULTD	F0	F2 F4	6	9	
SUBD	F8	F6 F2	7	9	11 12
DIVD	F10	F0 F6	8		
ADD	F6	F8 F2	13	14	16

Functional unit status		dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
2 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
Add	Yes Add	F6	F8	F2			No	No
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	17	FU									
		Mult1			Add		Divide				

Oct. 26, 2004

27

## Scoreboard Example Cycle 18

Instruction status			Read	Execu	Write
Instruction	j	k	Issue	operai	compl Result
LD	F6	34+ R2	1	2	3 4
LD	F2	45+ R3	5	6	7 8
MULTD	F0	F2 F4	6	9	
SUBD	F8	F6 F2	7	9	11 12
DIVD	F10	F0 F6	8		
ADD	F6	F8 F2	13	14	16

Functional unit status		dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No							
1 Mult1	Yes Mult	F0	F2	F4			No	No
Mult2	No							
Add	Yes Add	F6	F8	F2			No	No
Divide	Yes Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30	
Clock	18	FU									
		Mult1			Add		Divide				

Oct. 26, 2004

28

## Scoreboard Example Cycle 19

Instruction status			Read	Execu	Write	
Instruction	j	k	Issue	operat	compl	Result
LD	F6	34+ R2	1	2	3	4
LD	F2	45+ R3	5	6	7	8
MULTD	F0	F2 F4	6	9	19	20
SUBD	F8	F6 F2	7	9	11	12
DIVD	F10	F0 F6	8			
ADD	F6	F8 F2	13	14	16	

Functional unit status		dest	S1	S2	FU for	FU for Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj Rk
Integer	No						
Mult1	Yes Mult	F0	F2	F4			No No
Mult2	No						
Add	Yes Add	F6	F8	F2			No No
Divide	Yes Div	F10	F0	F6	Mult1		No Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	19	FU		Add		Divide				

Oct. 26, 2004

29

## Scoreboard Example Cycle 20

Instruction			j	k	Issue	operat	compl	Result
LD	F6	34+ R2	1	2	3	4		
LD	F2	45+ R3	5	6	7	8		
MULTD	F0	F2 F4	6	9	19	20		
SUBD	F8	F6 F2	7	9	11	12		
DIVD	F10	F0 F6	8					
ADD	F6	F8 F2	13	14	16			

Functional unit status		dest	S1	S2	FU for	FU for Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj Rk
Integer	No						
Mult1	No						
Mult2	No						
Add	Yes Add	F6	F8	F2			No No
Divide	Yes Div	F10	F0	F6			Yes Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	20	FU		Add		Divide				

Oct. 26, 2004

30

## Scoreboard Example Cycle 21

Instruction			j	k	Issue	operat	compl	Result
LD	F6	34+ R2	1	2	3	4		
LD	F2	45+ R3	5	6	7	8		
MULTD	F0	F2 F4	6	9	19	20		
SUBD	F8	F6 F2	7	9	11	12		
DIVD	F10	F0 F6	8	21				
ADD	F6	F8 F2	13	14	16			

Functional unit status		dest	S1	S2	FU for	FU for Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj Rk
Integer	No						
Mult1	No						
Mult2	No						
Add	Yes Add	F6	F8	F2			No No
Divide	Yes Div	F10	F0	F6			No No

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	21	FU		Add		Divide				

Oct. 26, 2004

31

## Scoreboard Example Cycle 22

Instruction			j	k	Issue	operat	compl	Result
LD	F6	34+ R2	1	2	3	4		
LD	F2	45+ R3	5	6	7	8		
MULTD	F0	F2 F4	6	9	19	20		
SUBD	F8	F6 F2	7	9	11	12		
DIVD	F10	F0 F6	8	21				
ADD	F6	F8 F2	13	14	16	22		

Functional unit status		dest	S1	S2	FU for	FU for Fj?	Fk?
Tim Name	Busy Op	Fi	Fj	Fk	Qj	Qk	Rj Rk
Integer	No						
Mult1	No						
Mult2	No						
Add	No						
Divide	Yes Div	F10	F0	F6			No No

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	21	FU		Divide						

Oct. 26, 2004

32

## Scoreboard Example Cycle 61

Instruction	<i>j</i>	<i>k</i>	Issue	operand	compl	Result
LD	F6	34+	R2	1	2	3 4
LD	F2	45+	R3	5	6	7 8
MULTD	F0	F2	F4	6	9	19 20
SUBD	F8	F6	F2	7	9	11 12
DIVD	F10	F0	F6	8	21	61
ADDD	F6	F8	F2	13	14	16 22

Functional unit status		dest	S1	S2	FU for i	FU for j?	Fk?			
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	Yes	Div	F10	F0	F6			No	No

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	61							Divide		

Oct. 26, 2004

33

## Scoreboard Example Cycle 62

Instruction status		Read	Executing	Write		
Instruction	<i>j</i>	<i>k</i>	Issue	operand	complete	Result
LD	F6	34+	R2	1	2	3 4
LD	F2	45+	R3	5	6	7 8
MULTD	F0	F2	F4	6	9	19 20
SUBD	F8	F6	F2	7	9	11 12
DIVD	F10	F0	F6	8	21	61 62
ADDD	F6	F8	F2	13	14	16 22

Functional unit status		dest	S1	S2	FU for j	FU for k?	Fk?			
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
	Mult1	No								
	Mult2	No								
	Add	No								
	Divide	No								

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	62									

Oct. 26, 2004

34

## Scoreboard Summary

### • Limitations of 6600 scoreboard:

- No forwarding hardware
- Limited to instructions in basic block (small *window*)
- Small number of functional units (structural hazards)
- Wait for WAR hazards
- Prevent WAW hazards

• Homework: A.13 on page A-86 Due on Oct. 24

Oct. 26, 2004

35