

Jun Yang

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RESEARCH INTERESTS

Secure microprocessors: architecture support for secure execution of software.
Thermal aware microarchitecture: efficient dynamic thermal management for processors.
Network processors: power performance tradeoffs for multi-core, multi-threaded processors.

PROFESSIONAL PREPARATION

- **Ph.D.** in Computer Science, University of Arizona, September 2002.
- **M.S.** in Computer Science, University of Pittsburgh, June 1999.
- **M.A.** in Applied Mathematics, Worcester Polytechnic Institute, August 1997.
- **B.S.** in Computer Science, Nanjing University, P. R. China, June 1995.

APPOINTMENTS

- Assistant Professor, Department of Computer Science and Engineering, University of California, Riverside, 2002–present.

PUBLICATIONS

Journal Publications

- ACM TACO Chuanjun Zhang, Frank Vahid, Jun Yang, and Walid Najjar “A Way-Halting Cache for Low-Energy High-Performance Systems,” *ACM Transactions on Architecture and Code Optimization*, Vol. 2, No. 1, pp. 34-54, March 2005.
- IEEE TC Jun Yang, Lan Gao, and Youtao Zhang, “Improving Memory Encryption Performance in Secure Processor,” *IEEE Transactions on Computers*, pp. 630-640, Vol. 54, No. 5, May 2005.
- JSA Jun Yang, Jia Yu, and Youtao Zhang, “A Low Energy Cache Design for Multimedia Applications Exploiting Set Access Locality,” *Journal of Systems Architecture*, Vol. 51, No. 10-11, October-November 2005.
- JEC Youtao Zhang, Jun Yang, “Reducing I-cache Energy of Multimedia Applications through Low Cost Tag Comparison Elimination,” *Journal of Embedded Computing*, No. 4, July 2005.
- IEEE MICRO Yan Luo, Jun Yang, and Laxmi Bhuyan, “NePSim: A Network Processor Simulator with Power Evaluation Framework,” *IEEE Micro Magazine*, special issue on network processors for future high-end systems and applications, September–October, 2004.

- ACM TODAES Jun Yang, Rajiv Gupta and Chuanjun Zhang, "Frequent Value Encoding for Low Power Data Buses," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 9, No. 3, July 2004.
- CAL Chuanjun Zhang, Frank Vahid, Jun Yang, and Walid Najjar, "A Way-Halting Cache for Low-Energy High-Performance Systems," *Computer Architecture Letters*, Vol. 2, September 2003.
- ACM TECS Jun Yang and Rajiv Gupta, "Frequent Value Locality and its Applications," *ACM Transactions on Embedded Computing Systems*, special inaugural issue on memory systems, Vol. 1, No. 1, pp. 79–105, November 2002.
- JBE'99 Dalin Tang, Jun Yang, Chun Yang and David N. Ku, "A Nonlinear Axisymmetric Model with Fluid-Wall Interactions for Viscous Flows in Stenotic Elastic Tubes," *Journal of Biomechanical Engineering*, Vol. 121, pp. 494-501, 1999.
- JSC'00 Dalin Tang and Jun Yang, "A Free Moving Boundary Model and Boundary Iteration Method for Unsteady Viscous Flow in Stenotic Elastic Tubes," *SIAM Journal on Scientific Computing*, Vol. 21, No. 4, pp. 1370-1386, 2000.
- Conference and Refereed Workshop Publications**
- HPCA12 Larry Shi, Josh Fryman, Hsien-Hsin S. Lee, Youtao Zhang and Jun Yang, "InfoShield: A Security Architecture for Protecting Information Usage in Memory," to appear, the 12th International Symposium on High-Performance Computer Architecture, Austin, TX, February, 2005.
- ICISS Lingling Jin, Wei Wu, Jun Yang, Chuanjun Zhang, Youtao Zhang, "Dynamic Co-allocation of Resources for Level One Caches," to appear, the 2nd International Conference on Embedded Software and Systems, Xian, China, December 2005.
- HiPEAC'05 Jia Yu, Jun Yang, Shaojie Chen and Yan Luo, "Enhancing Network Processor Simulation Speed With Statistical Input Sampling," to appear, 2005 International Conference on High Performance Embedded Architectures & Compilers, Barcelona, Spain, 17-18 November 2005.
- ICCAD'05 Pu Liu, Zhenyu Qi, Hang Li, Lingling Jin, Wei Wu, Sheldon X.-D. Tan and Jun Yang, "Fast Thermal Simulation for Architecture Level Dynamic Thermal Management," to appear, International Conference on Computer-Aided Design, San Jose, November 2005.
- ICCD'05 Hang Li, Pu Liu, Zhenyu Qi, Lingling Jin, Wei Wu, Sheldon X.-D. Tan and Jun Yang, "Efficient Thermal Simulation for Run-Time Temperature Tracking and Management," to appear, International Conference on Computer Design (short paper), San Jose, October, 2005.
- ICCD'05 Dinesh Suresh, Banit Agrawal, Walid Najjar and Jun Yang "VALVE: Variable Length Value Encoding for Off-Chip Data Buses," to appear, International Conference on Computer Design, San Jose, October, 2005.
- ISLPED'05 Dinesh Suresh, Banit Agrawal, Walid Najjar and Jun Yang, "Tunable Bus Encoder for Off-Chip Data Buses," *International Symposium On Low Power Electronics and Design*, pp. 319-322, August 2005.
- DAC42 Yan Luo, Jia Yu, Jun Yang and Laxmi Bhuyan, "Low Power Network Processor Design Using Clock Gating," *The 42nd Annual Conference on Design Automation*, pp. 712-715, June 2005.
- DATE'05 Jia Yu, Wei Wu, Xi Chen, Harry Hsieh, Jun Yang, F. Balarin, "Assertion-Based Automatic Design Exploration of DVS in Network Processor Architectures,"

- Design, Automation and Test in Europe 2005*, pp. 92-97, Vol. 1, March, 2005.
- HPCA11 Youtao Zhang, Lan Gao, Jun Yang, Xiangyu Zhang, Rajiv Gupta, "SENS: Security Enhancement to Symmetric Shared Memory Multiprocessors," *The 11th International Symposium on High-Performance Computer Architecture*, pp. 352-362, February, 2005.
- SAC Yongjing Lin, Youtao Zhang, Quanzhong Li, and Jun Yang, "Supporting Efficient Query Processing on Compressed XML Files," *ACM The 20th Annual Symposium on Applied Computing*, pp. 660-665, March, 2005.
- WASSA Youtao Zhang, Jun Yang, Yongjing Lin, Lan Gao, "Architectural Support for Protecting User Privacy on Trusted Processors," *The Workshop on Architectural Support for Security and Anti-Virus, In conjunction with the 11th ASPLOS*, pp. 114-119, October, 2004.
- ISLPED'04 Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar, "A Way-Halting Cache for Low-Energy High Performance Systems," *IEEE International Symposium on Low Power Electronics and Design*, pp. 126-131, August, 2004.
- DATE'04 Chuanjun Zhang, Jun Yang, and Frank Vahid, "Low Static Power High Performance Frequent Value Data Caches," *Design, Automation and Test in Europe*, Paris, France, February 2004.
- MICRO36 Jun Yang, Youtao Zhang, and Lan Gao, "Fast Secure Processor for Inhibiting Software Piracy and Tampering," *ACM/IEEE 36th International Symposium on Microarchitecture*, pp. 351-360, December 2003.
- HiPC10 Dinesh Suresh, Jun Yang, Chuanjun Zhang, Banit Agrawal, Walid Najjar, "Reducing Transition Activity on Data Bus," *The 10th Annual International Conference on High Performance Computing*, pp. 44-54, December 2003.
- CASES'03 Dinesh Suresh, Banit Agrawal, Jun Yang, Walid Najjar, and Laxmi Bhuyan, "Power Efficient Encoding Techniques for Off-chip Data Buses," *2003 International Conference on Compilers, Architecture and Synthesis for Embedded Systems*, pp. 267-275, October 2003.
- ICPP'03 Youtao Zhang and Jun Yang, "Procedural Level Address Offset Assignment of DSP Applications with Loops," *International Conference on Parallel Processing*, pp. 21-28, October 2003.
- ISLPED'03 Jun Yang, Jia Yu, and Youtao Zhang, "Lightweight Set Buffer: Low Power Data Cache for Multimedia Applications," *ACM/IEEE International Symposium on Low Power Electronics and Design*, pp. 270-273, 2003.
- ISLPED'03 Youtao Zhang, Jun Yang, "Low Cost Instruction Cache Design for Tag Comparison Elimination," *ACM/IEEE International Symposium on Low Power Electronics and Design*, pp. 266-269, 2003.
- MICRO'02 Jun Yang and Rajiv Gupta, "Energy Efficient Frequent Value Data Cache Design," *ACM/IEEE 35th International Symposium on Microarchitecture*, pages 97-107, Istanbul, Turkey, November 2002.
- ISLPED'01 Jun Yang and Rajiv Gupta, "FV Encoding for Low-Power Data I/O," *ACM/IEEE International Symposium on Low Power Electronics and Design*, pages 84-87, August 2001.
- ISLPED'01 Jun Yang and Rajiv Gupta, "Energy-Efficient Load and Store Reuse," *ACM/IEEE International Symposium on Low Power Electronics and Design*, pages 72-75, August 2001.

MICRO'00	Jun Yang, Youtao Zhang and Rajiv Gupta, "Frequent Value Compression in Data Caches," <i>ACM/IEEE 33rd International Symposium on Microarchitecture</i> , pages 258–265, December 2000.
ASPLOS'00	Youtao Zhang, Jun Yang and Rajiv Gupta, "Frequent Value Locality and Value-Centric Data Cache Design," <i>ACM 9th International Conference on Architecture Support for Programming Languages and Operating Systems</i> , pages 150–159, November 2000.
ICPP'00	Jun Yang and Rajiv Gupta, "Load Redundancy Removal through Instruction Reuse," <i>International Conference on Parallel Processing</i> , pages 61–68, August 2000.

GRANTS

- National Science Foundation, Computing Processes & Artifact, *Collaborative Research: Architectural Support for Security and Privacy Protection on Uni- and Multi- Processors*, CCF-0430021, UCR budget \$54,001, 11/2004-10/2005.
- Academic Senate Research Funds, UCR 2003-2004.
- Regent's Faculty Fellowship/Faculty Development Award, UCR 2003-2004.

SYNERGISTIC ACTIVITIES

- **Vice Chair**
 1. Embedded System Architecture track, The International Conference on Embedded And Ubiquitous Computing (EUC) Seoul, Korea in August 2006.
- **Technical Program Committee Member**
 1. The 2nd International Conference on Embedded Software and Systems, December, 2005.
 2. ACM SIGPLAN/SIGBED 2005 Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES'05), June 2005
 3. 10th International Conference on High Performance Computing (HiPC), Hyderabad, India, December 2003.
- **Panel**

NSF Cyber Trust, April 2005.
- **Reviewer for Conferences/Journals**

MICRO, HPCA, PLDI, LCTES, CASES, HiPC, DATE, ISSS-CODES, ACM TODAES, ACM TACO, IEEE TC, IEEE TPDS, IEEE TVLSI.
- **Membership**

ACM, ACM SIGARCH, IEEE

PH.D. STUDENTS

- Yan Luo (co-advised with Laxmi Bhuyan) – Assistant Professor (2005-), University of Massachusetts Lowell.