UC RIVERSIDE UNIVERSITY OF CALIFORNIA

Curriculum Vitae

Joseph Tarango

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Objective: Research/Production position in embedded, hardware, and/or software development of standalone or integrated systems.

Research Interests: Computer architecture, embedded systems, optimization of integrated systems, and reconfigurable computing.

EDUCATION

University of California, Riverside — December 2015 (Expected)
Ph.D. Computer Science & Engineering

University of California, Riverside —December 2012
M.S. Computer Engineering

University of California, Riverside — June 2010
B.S. Computer Engineering

Crafton Hills College — June 2007
A.S. Mathematics
A.S. Physics

Pertinent Engineering Experience:

A-plus (A+), Apprentice Teaching, Algorithms and Data Structures, Automata and Formal Languages, Assembly Programming, Advanced Computer Architecture, Advanced Computer Networks, Compiler Construction, Computer-Aided Electronic Circuit Simulation, Data Mining Techniques, Design and Architecture of Computer Systems, Design of Operating Systems, Digital Circuit Design, Discrete Structures, Electronic Circuits, Embedded and Real-Time Systems, Logic Design, Machine Organization, Modeling and Simulation, NAND Memory, Network Routing, Phase Change Memory, Signal and Systems, Software and Hardware Engineering of Embedded Systems, Software Engineering, Solid State Electronics, Synthesis of Digital Systems, Reconfigurable Computing, Technical Communications, and Testing & Verification Techniques

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TECHNICAL EXPERTISE

Programming Languages	C, C++, Perl, Python, and VHDL
Design Software	Altera, Cadence, Green Hills Software, PSPICE, Synopsys, Synplify, and Xilinx
Operating Systems / Platforms	DOS, Windows, and UNIX.

PROFESSIONAL EXPERIENCE

Employment:

- *Intel Corporation:* Intel Technology and Manufacturing group in Longmont, CO. Senior Firmware Engineer in Non-Volatile Memory Systems Group (NSG). (2013-Present)

Internships:

- *University of Bern:* Under the guidance of Dr. Theo Kluter; worked on the VHDL implementation of (RISC) soft processor and compilation tool chain. (2011)
- *National University of Singapore:* Under the guidance of Dr. Tulika Mitra; Developed reconfigurable customized processor data paths based on detailed hot sequences within encryption, media, SPEC benchmarks. Reconfigurable custom datapaths were developed to interface with ARM Cortex-A9 processors and SimpleScalar. (2012)
- *Intel Corporation:* Intel Technology and Manufacturing group in Longmont, CO. Worked with Intel Engineers to enhance Solid State Drive (SSD) performance. (2013)

Leadership:

- *Director:* Organized and prepared teams for Association of Computing Machinery programming competition. I instructed teams on optimal communication techniques and how to efficiently code algorithms in C++.

Professional service and consultations:

- *Consultant:*Worked with Jacquard Computing Inc. to build VHDL interfaces for FPGA platforms.

Projects:

- *Design Project:* Designed a multi-stage audio amplifier from MOSFETs/BJTs to augment a small signal input to a high power audio system. The stages included a: differential input, voltage amplification, and push-pull output.
- *Implementation:* Updated program interface for a reduced instruction set computer (RISC) soft-processor on a Custom Field Programmable Gate Array (FPGA) for Dr. Phillip Brisk (UC Riverside Professor).

Publications:

[CODES+ISSS] Instruction Set Extensions for Dynamic Time Warping

J. Tarango, E. Keogh, and P. Brisk International Conference on Hardware/Software Codesign and System Synthesis Montreal, Canada, September 29 -October 4, 2013.

[ICCAD] A Just-in-Time Customizable Processor

L. Chen, J. Tarango, T. Mitra, and P. Brisk International Conference on Computer-Aided Design San Jose, CA, USA, November 18-21, 2013

[ASILOMAR-SSC] Accelerating the Dynamic Time Warping Distance Measure using Logarithmic Arithmetic

J. Tarango, E. Keogh, and P. Brisk
Pacific Grove, CA, November 2-5, 2014

Teaching:

University of California, Riverside

- *Teaching Assistant:* CS5 Introduction to Computer Programming, Winter 2011
- *Teaching Assistant:* CS61 Machine Organization and Assembly Language Programming, Spring 2011
- *Teaching Assistant:* CS120B Introduction to Embedded Systems, Summer 2011
- *Teaching Assistant:* CS122A Intermediate Embedded and Real-Time Systems, Fall 2011
- *Teaching Assistant:* CS120B Introduction to Embedded Systems, Winter 2012
- *Teaching Assistant:* CS8 Introduction to Computing, Spring 2012
- *Teaching Assistant:* CS161 Design and Architecture of Computer Systems, Spring 2012
- *Teaching Assistant:* CS161L Design and Architecture of Computer Systems, Spring 2012

Research:

- *Research:* Research Assistant for Dr. Walid Najjar (UC Riverside Professor) on Riverside Optimizing Compiler for Configurable Computing (ROCCC). ROCCC is a C to VHDL compiler, which enables C programs to be translated to a high-speed FPGA platform. My work included building generalized VHDL interfaces for the Pico E-16 FPGA to work with ROCCC.
- *Current Research:* Arithmetic optimization through compiler and hardware accelerators; the projects included prototyping algorithms to run on tightly coupled FPGA and computing systems.

INVOLVEMENT

Memberships and Associations	Member, Association of Computing Machinery
	Member, Institute of Electronics and Electrical Engineers
	Member, Society of Hispanic Professional Engineers
	Member, Alpha Gamma Sigma Honor Society

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Fellowships

Alliance for Graduate Education and the Professoriate Fellow
CCRAA Fellow
Dean's Distinguished Fellow
NSF EASPI Fellow

Significant Awards

Diversity Award
EOPS/CARE/CalWorks Scholar Award
Hispanic Scholar Award

Volunteer Experience

Crafton Hills Aid for Unfortunate Families
Joslyn Senior Center in Redlands, California
Math Tutor at Fontana High School and Crafton Hills College
MESA Day
Redlands High School Wrestling Team
Special Olympics of Southern California
UCR Bourns College of Engineering Family Night

Special Events

Graduate Research Day (Sacramento, CA 2013)

Special Presentations

A Just-in-Time Customizable Processor (UCR AGEP 2013)
Accelerating Time-series Subsequences Using Instruction Set Extensions for Embedded Systems (UCR AGEP 2013)

References

Available upon request

Last updated: March 26, 2015