

CS220
Synthesis of Digital Systems
 Harry Hsieh
 Department of Computer Science and Engineering
 University of California at Riverside

CS220: Synthesis of Digital Systems

- Class Meeting
 - Engineering Unit II, Room 315
 - TuTh 9:40AM-11AM
- Prerequisite:
 - CS/EE 120B, CS 161, CS 141
 - Or, graduate standing
 - Plus, consent of instructor
- 4 units, grades only
- Midterm (10/31, in class)
- Final (12/7, in class)

• www.cs.ucr.edu/~harry/cs220

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Instructor

- Harry Hsieh
 - www.cs.ucr.edu/~harry
 - harry@cs.ucr.edu
 - Office (827-2030)
 - Engineering Unit II, Room 339
 - TueWed 11AM-noon
 - Check www for cancellation
 - Also available
 - by appointment

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Textbooks

- Recommended:
 - Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits". McGraw Hill, 1994, ISBN:0-07-016333-2
- Available in library on 1 day reserve
- Extra hand-outs will be available throughout the quarter.
- You will only be responsible with material covered in class

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Grades

- Examinations 60%
 - Midterm1/Midterm2 breakdown TBA
 - Likely: 40% midterm1, 20% midterm2
 - Not cumulative
 - Close everything
- Project 20%
 - Individual
 - 2 presentations
 - 1 final report
- Homework 15%
 - May work in groups
 - Must do your own write-up
 - Late homework will be penalized

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Grades

- 85/70/60/50 rule
 - 85%-100% A
 - 70%-85% B
 - 60%-70% C
 - 50%-60% D
- Everyone can get A's
 - And often does
- Curve may be applied
 - Only to help the grades

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What's to be covered

- Once-over of current techniques in silicon compilation (3/4 of the course)
 - Hardware modeling
 - Architectural synthesis
 - Scheduling algorithms
 - Resource sharing and binding
 - Two-level combinational logic optimization
 - Multiple-level combinational logic optimization
 - Sequential logic optimization
 - Cell library binding
- Advance Topic (1/4 of the course)
 - Designing multimedia applications with process networks
 - Implementing MPSoC with platform FPGA
 - Communication synthesis for modern VLSI
 - Behavioral - RTL correlation
 - System level design space exploration
 - Property verification





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Research-Project

- 1 "progress" presentation: 11/2
- 1 final presentation: 12/5
- 4 page final report
 - Conference format: double column, single space...
- Can be related to your research topic
 - List available 10/3
 - Must pick one by 10/10

As much (or as little) as you made of it !!!






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Research-Project (cont.)

- Minimum requirement
 - 1st presentation:
 - initial literature survey and problem definition
 - Final presentation:
 - complete literature survey plus proposed solution
- A+ work
 - 1st presentation
 - Complete literature survey plus proposed solution
 - Final presentation
 - Implemented solution with result table





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Projects

- MPSoC
 - System level performance analysis using compiled simulation
 - Implementing mpeg-2 decoder on microblaze FPGA
 - Communication synthesis: queue, memory, or network?
- Behavioral - RTL correlation
 - Correlation of combinational signals
 - Correlation checking of behavioral - RTL registers
- Your own proposed project!




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Homework and Discussion

- 4 homeworks (15%)
 - You are encouraged to work with each other
 - But do your own write up
- Attendance (5%)
 - Unexcused absence will be penalized
- Discussion
 - Encouraged



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Synthesis of Digital Systems

9/28/2006

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What this class is all about...

- Electronic Design Automation
 - Physical (EE260)
 - Logic-Level (CS220)
 - Architectural-Level (CS220)
 - System-Level (CS269)

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Microelectronics

- Enabling technology for digital systems
- Market categories:
 - Information Systems
 - E.g. computers
 - Telecommunications
 - E.g. cell phone
 - Consumer
 - E.g. camera
 - Transportation systems
 - E.g. ABS
 - Manufacturing systems
 - E.g. robots

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Time, Time, Time,...

- Time to market is the most important metric
 - 6 month between generations of cellphones

- Computer Aided Design (CAD)
 - Enabling technology for microelectronics
 - Large scale design management
 - Design optimization
 - Design validation

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Trends in Microelectronics

Year	Processor	Transistors
1978	8086	29,000
1982	286	120,000
1985	386	275,000
1989	486	1,180,000
1993	Pentium	3,100,000
1997	Pentium II	7,500,000
1999	Pentium III	24,000,000
2000	Pentium IV	42,000,000

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Microelectronic design styles

- Custom
 - High volume, high performance, lay down gate-by-gate.
 - E.g. parts of general purpose processors (e.g. instruction fetch)
- Semi-custom
 - Cell-based
 - Standard-cells
 - Macro-cells
 - Memory generators
 - PLA generators
 - Array-based
 - Pre-diffused Gate arrays
 - Sea of gates
 - Pre-Wired Anti-fuse based Memory-based

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Standard cells

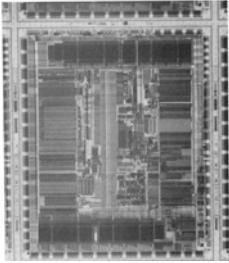
- Cell library
 - Designed cells once
 - Highly optimized cells
- Layout styles:
 - Cells are placed in rows
 - Channels are used for wiring
- Compatible with custom design

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Macro-cells

- Module generators:
 - Synthesize layout
 - Variable area and aspect-ratio
- Examples
 - RAM, ROM, PLA...
- Layout can be highly optimized
- Maybe hard to route

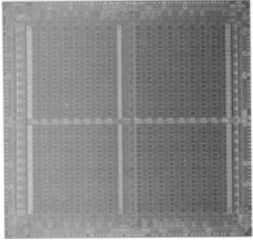


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Field Programmable Gate Arrays

- Array of cells
 - Each cell performs a logic function
- Personalization
 - Soft: memory cell
 - Hard: anti-fuse
- Immediate turn-around
 - Programmed in field
- Relative low performance and density
- Not all gate arrays are field programmable (lower cost)



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Trade-offs

	Custom	Cell-Based	FPGA
Density	Very High	High	Medium-low
Performance	Very High	High	Medium-Low
Flexibility	Very High	High	Low
Design Time	Very Long	Short	Very Short
Manufacturing Time	Medium	Medium	Very Short
Cost - low volume	Very High	High	Low
Cost - high volume	Low	Low	High

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Microelectronic circuit design activities

- Conceptualization and modeling:
 - Hardware description languages (VHDL, Verilog)
 - Software languages (C, C++)
 - System level languages (SystemC)
- Synthesis and optimization
 - Refinement
 - E.g. HDL->Gate->Transistors
- Validation
 - Simulation
 - Formal verification
 - Property verification
 - Equivalence Checking

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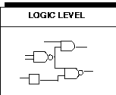
Modeling abstraction

- Architectural level
 - Operations, data computation, transfer
- Logic level
 - Logic functions
- Geometrical level:
 - Geometrical objects

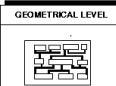
ARCHITECTURAL LEVEL

... PC = PC + 1;
FETCH (PC);
DECODE (RHS);
...

LOGIC LEVEL



GEOMETRICAL LEVEL



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View classification: Y-chart

Structural

Processors, memories

Registers, FUs, MUXs

Gates, flip-flops

Transistors

Behavior

Sequential programs

Register transfers

Logic equations/FSM

Transfer functions

- Axis represents "views"
 - Behavioral
 - Defines outputs as function of inputs
 - Algorithms but no implementation
 - Structural
 - Implements behavior by connecting components with known behavior
 - Physical
 - Gives size/locations of components and wires on chip/board

Cell Layout

Modules

Chips

Boards

Physical

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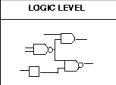
Circuit Synthesis

- Architectural-level synthesis
 - Determine the macroscopic structure
 - Interconnection of major building blocks
- Logic-level synthesis
 - Determine the microscopic structure
 - Interconnection of logic gates
- Geometrical-level synthesis
 - Determine position and connections
 - Physical design

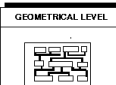
ARCHITECTURAL LEVEL

...
PC ← PC + 1;
FETCH (PC);
DECODE (NEXT);
...

LOGIC LEVEL



GEOMETRICAL LEVEL



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Y-chart

Structural

Processors, memories

Registers, FUs, MUXs

Gates, flip-flops

Transistors

Behavior

Sequential programs

Register transfers

Logic equations/FSM

Transfer functions

- Synthesis converts behavior at given level to structure at same level or lower
 - E.g.,
 - Sequential Program → gates, flip-flops
 - Sequential Program → transistors

Cell Layout

Modules

Chips

Boards

Physical

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