

Administrative Matters

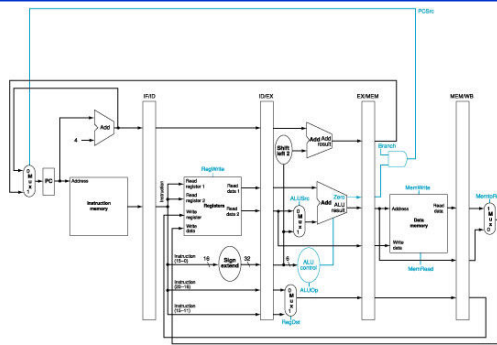
- Homework #5
 - Will be posted today
 - Due Friday 11/16 at 2PM through moodle
- Midterm #2
 - Monday, 11/19
 - Cover chapter 5 and 6
 - Cover homework 4 and 5
 - 15% of your grade
- No class on Monday 11/12
 - Happy Veteran's Day



Chapter Six

Enhancing Performance with Pipelining (continue)

Adding control to pipelined datapath

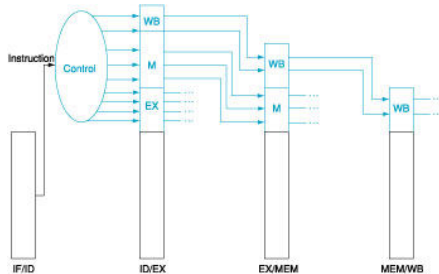


Control

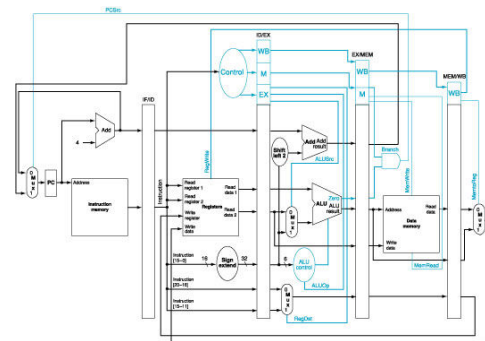
- How to control depends on what instruction is at that stage

Instruction	Execution/Address Calculation stage control lines				Memory access stage control lines			stage control lines	
	Reg Dst	ALU Op1	ALU Op0	ALU Src	Branch	Mem Read	Mem Write	Reg write	Mem to Reg
R-format	1	1	0	0	0	0	0	1	0
lw	0	0	0	1	0	1	0	1	1
sw	X	0	0	1	0	0	1	0	X
beq	X	0	1	0	1	0	0	0	X

Passing the control signal from stage to stage

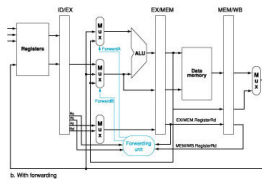
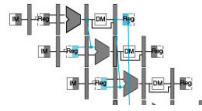


Datapath with Control



Quick Questions

- If we have
 - add \$1, \$1, \$2
 - add \$1, \$1, \$3
 - add \$1, \$1, \$4
- Where will \$1 be coming from?



Quick question

- What else is wrong?
- What about immediate?

