

UCR CS122A, Fall 2003
Embedded System Design
Prof. Harry Hsieh
Homework #5

Due December 4th, at the beginning of the class

1. (20 points) Given a function $F=(x+y)'$.
 - a. Draw the CMOS circuit schematic. Clearly draw the PMOS and NMOS transistors.
 - b. Draw the top-down view of the circuit on an IC (make your layout as compact as possible)
2. (5 point) What term is used to refer to sending IC design to the manufacturing foundry?
3. (5 point) What term is used to refer to one time through the manufacturing process?
4. (30 points) Given the logic equation $F(a,b,c)=ac'+a'c+ab'c+a'bc'$
 - a. How many literals are there in the representation?
 - b. List all minterms of the function.
 - c. List all implicants of the function.
 - d. List all prime implicants of the function.
 - e. What is the minimum cover of the function?
 - f. Is there more than one different minimum cover? If so, what is another minimum cover representation?
5. (10 points) Draw Gasjki's Y-chart, label each axis, and list four abstraction levels on each axis.
6. (5 points) In simulation, what is the term used to refer to the ability to direct and affect a system's execution?
7. (5 points) In simulation, what is the term used to refer to the ability to see system value?
8. (5 points) Behavior Synthesis usually starts from:
 - a. Gate level description yes___no___
 - b. Logic description yes___no___
 - c. Sequential program yes___no___
 - d. Process network yes___no___
 - e. RTL description yes___no___
9. (5 points) Physical Design usually starts from:
 - a. Gate level description yes___no___
 - b. Logic description yes___no___
 - c. Sequential program yes___no___
 - d. Process network yes___no___
 - e. RTL description yes___no___

10. (5 point) Logic synthesis usually starts from:
- a. Gate level description yes ___ no ___
 - b. Logic description yes ___ no ___
 - c. Sequential program yes ___ no ___
 - d. Process network yes ___ no ___
 - e. RTL description yes ___ no ___
11. (5 point) System synthesis usually starts from:
- a. Gate level description yes ___ no ___
 - b. Logic description yes ___ no ___
 - c. Sequential program yes ___ no ___
 - d. Process network yes ___ no ___
 - e. RTL description yes ___ no ___