

VITA
RAJIV GUPTA

University of California, Riverside
Computer Science & Engineering
Winston Chung Hall, Room 408
Riverside, CA 92521

www.cs.ucr.edu/~gupta
✉ gupta@cs.ucr.edu
☎ 951-827-2558
📞 949-419-6659

RESEARCH INTERESTS

High-Performance Computing: Programming, Compiler, Runtime, and Architectural Support;
Scalable Irregular Big Data Processing on GPGPU-based Heterogeneous Clusters;
Software Tools for Monitoring, Analysis, Debugging, and Slicing of Parallel Programs.

EDUCATION

Ph.D. in Computer Science, University of Pittsburgh, PA, Aug. 1987 (Advisor: Prof. M.L. Soffa).
M.S. in Computer Science, University of Pittsburgh, PA, April 1984 (Advisor: Prof. M.L. Soffa).
B.Tech. in Electrical Engineering, Indian Institute of Technology, New Delhi, India, April 1982.

APPOINTMENTS

Distinguished Professor, Dept. of Comp. Science & Engr., UC Riverside, 7/2017 - present.
Professor, Dept. of Comp. Science & Engr., Univ. of California Riverside, 8/2007 - 6/2017.
Professor, Department of Computer Science, The University of Arizona, 8/1999 - 8/2007.
Professor, Department of Computer Science, University of Pittsburgh, 9/1998 - 8/1999.
Associate Professor, Dept. of Computer Science, University of Pittsburgh, 9/1994 - 8/1998.
Faculty Member, Computer Engineering Program, University of Pittsburgh, 9/1997 - 8/1999.
Visiting Faculty, Microprocessor Research Lab, Intel Corporation, 9/1996 - 12/1996.
Assistant Professor, Dept. of Computer Science, University of Pittsburgh, 9/1990 - 8/1994.
Senior Member Research Staff, Philips Laboratories, Briarcliff Manor, NY, 10/1987 - 8/1990.
Research/Teaching Assistant, Dept. of Comp. Science, Univ. of Pittsburgh, 9/1982 - 8/1987.

AWARDS AND HONORS

Technical Advisory Group

- Member, *Technical Advisory Group* on **Networking and Information Technology** for the **US President's Council of Advisors in Science and Technology**, May 2006 – Sept. 2007.

Research (h-index = 58 → <https://scholar.google.com/citations?user=6P4bGWAAAAAJ>)

- **ACM Fellow** (2009) - *for contributions to program analysis and optimization and sustained professional service to the computer science research community.*
- **IEEE Fellow** (2008) - *for contributions to computer architecture and optimizing compilers.*

- **AAAS Fellow** (2011) - *for contributions to computer architecture and optimizing compilers.*
- **UCR Doctoral Dissertation Advisor/Mentor Award**, 2012.
- **LCPC 2015 Best Student Paper Award**: “Size Oblivious Programming with *InfiniMem*,” *International Workshop on Languages and Compilers for Parallel Computing*, Sept. 2015.
- **PACT 2010 Best Paper Award**: “Efficient Sequential Consistency Using Conditional Fences,” *International Conference on Parallel Architectures and Compilation*, September 2010.
- **ICSE 2003 Distinguished Paper Award**: “Precise Dynamic Slicing Algorithms,” *International Conference on Software Engineering*, May 2003.
- **Most Influential Papers of PLDI 1979-1999**: “Complete Removal of Redundant Computations,” *ACM SIGPLAN Conference on Programming Language Design and Implementation*, June 1998. Reprint and retrospective in *20 Years of PLDI (1979-1999): A Selection*, 2004.
- **ICPP 2003 Most Original Paper Award**: “Enabling Partial Cache Line Prefetching Through Data Compression,” *International Conference on Parallel Processing*, October 2003.
- **ICECCS 1996 Outstanding Paper Award**: “Designing a Non-intrusive Monitoring Tool for Developing Complex Distributed Applications,” *Second IEEE International Conference on Engineering of Complex Computer Systems*, Montreal, Canada, October 1996.
- *Dissertation Advisor of ACM SIGPLAN Outstanding Doctoral Dissertation Award winners*:
 - Rastislav Bodik, *Path and Value Sensitive Code Optimizations*, 2001.
 - Xiangyu Zhang, *Fault Location Via Precise Dynamic Slicing*, 2006.
- **Presidential Young Investigator Award**, National Science Foundation, 1991.
- **Faculty Impact Award**, CS Department, The University of Arizona, 2006 and 2007.
- **Making a Difference Award**, Philips Laboratories, Briarcliff Manor, New York, 1988.
- **Andrew Mellon Predoctoral Fellow**, FAS, University of Pittsburgh, Pittsburgh, PA, 1985.

Teaching: Obtained the highest student evaluation score among CS faculty teaching:

- a graduate core course during academic year 1995-1996, University of Pittsburgh.
- an advanced graduate elective during academic year 1995-1996, University of Pittsburgh.
- a graduate core course during academic year 1994-1995, University of Pittsburgh.

Service

- **ACM Recognition of Service Award** for serving as the General Chair for ASPLOS 2011.
- **ACM Recognition of Service Award** for serving as the General Chair for PLDI 2008.
- **ACM Recognition of Service Award** for serving as the Program Chair for LCTES 2005.
- **ACM Recognition of Service Award** for serving as the General Chair for CGO 2005.
- **ACM Recognition of Service Award** for serving as the Program Chair for PLDI 2003.
- **Recognition of Contributions and Leadership** at HiPC 2004.
- **ACM Recognition of Service Award** for serving as the Workshops Chair for ICS 2002.
- **IEEE Distinguished Visitor**, IEEE Computer Society, 2000-2002.

PROFESSIONAL ACTIVITIES

Associate Editor

- (PARCO) *Parallel Computing*, North Holland, 1991 – present.
- (COLA) *Journal of Computer Languages*, Elsevier, 2019 – present.
- (TACO) *ACM Transactions on Architecture and Code Optimization*, 2003 – 01/2017.
- (IEEE TC) *IEEE Transactions on Computers*, 2009 – 2014.
- (COMLAN) *Computer Languages, Systems and Structures*, Elsevier, 2006 – 12/2018.
- (JEC) *Journal of Embedded Computing*, 2003 – 2011.
- (IJPDSN) *IASTED Intl. Journal of Parallel and Distributed Systems and Networks*, 1996-2002.

Guest Editor

- (TECS) *ACM Transactions on Embedded Computing Systems*, special issue of on Language, Compiler, and Tool Support for Embedded Systems, Vol. 6, No. 4, September 2007.

Steering Committee Chair

- (FCRC 2016-2019) *ACM Federated Computing Research Conference*.
- (ASPLOS 2012-2013) *SIGPLAN/SIGOPS International Conference on Architectural Support for Programming Languages and Operating Systems*.
- (LCTES June 2006-September 2009) *ACM SIGPLAN Conference on Language, Compiler, and Tool Support for Embedded Systems*.

General Chair

- (FCRC 2015) *ACM Federated Computing Research Conference*, Portland, Oregon.
- (ASPLOS 2011) *ACM SIGPLAN/SIGOPS International Conference on Architectural Support for Programming Languages and Operating Systems*, Newport Beach, California.
- (PLDI 2008) *ACM SIGPLAN Conference on Programming Language Design and Implementation*, Tucson, Arizona.
- (CGO 2005) *IEEE/ACM International Symposium on Code Generation and Optimization*, San Jose, California (Co-Chair with Jesse Z. Fang).

Program Chair

- (AGP 2017) *First International Workshop on Architecture for Graph Processing*, held in conjunction with ISCA, (Co-Chair with Xuehai Qian).
- (ICISS 2014) Track Chair, Design Methodology and Tools, *IEEE International Conference on Embedded Software and Systems*.
- (CC 2010) *International Conference on Compiler Construction*.
- (HiPEAC 2008) *International Conf. on High-Performance Embedded Architectures and Compilers*. (Co-Chair with Minolis Katevenis)
- (LCTES 2005) *ACM SIGPLAN Conference on Language, Compiler, and Tool Support for Embedded Systems*.
- (PLDI 2003) *SIGPLAN Conference on Programming Language Design and Implementation*.
- (HPCA 2003) *IEEE International Symposium on High Performance Computer Architecture*.
- (HiPC 2003) Program Vice-Chair, Computer Architecture Track, *International Conference on High Performance Computing*.

- (ADCOM 2000) *Advanced Computing and Communication*. (Co-Chair with B.P. Sinha).
- (Dagstuhl Seminar) *Code Optimisation: Trends, Challenges, and Perspectives*, Dagstuhl, Germany, 2000 (Co-Chair with Jens Knoop, Carole Dulong, and Robert Kennedy).
- *First Workshop on Profile and Feedback-Directed Compilation*, held in conjunction with PACT, 1998 (Co-Chair with Brad Calder and James Larus).
- (LCT-RTS 1997) *ACM SIGPLAN Workshop on Language, Compiler, and Tool Support for Real-Time Systems*, held in conjunction with PLDI, (Co-Chair with David Whalley).

Registration Chair

- (PACT 2005) *International Conference on Parallel Architectures and Compilation Techniques*.

Workshops Chair

- (ASPLOS 2018) *ACM International Conference on Architectural Support for Programming Languages and Operating Systems* (Co-Chair with Zhijia Zhao).
- (ICS 2002) *ACM International Conference on Supercomputing*.

Steering Committee Member

- (ASPLOS 2011-2012) *ACM International Conference on Architectural Support for Programming Languages and Operating Systems*.
- (ETAPS 2010-2011) *The European Joint Conferences on Theory and Practice of Software*.
- (PLDI 2003-2005,2007-2010) *ACM SIGPLAN Conference on Programming Language Design and Implementation*.
- (HiPEAC 2005-2009) *International Conference on High-Performance Embedded Architectures and Compilers*.
- (HPCA 2003) *IEEE International Symposium on High Performance Computer Architecture*.
- (LCTES 2000-2010) *ACM SIGPLAN Conference on Language, Compiler, and Tool Support for Embedded Systems* (Member-at-large 2003-2005).

Selection Committee Member

- (IEEE Fellows), Member of IEEE CS Fellows Evaluation Committee [2008, 2009, 2010, 2012, 2013, 2014, 2015].
- (Most Influential PLDI 2008 Paper Award), Member of the Selection Committee [2018].
- (Most Influential PLDI 2003 Paper Award), Member of the Selection Committee [2013].
- (Most Influential PLDI 1994 Paper Award), Member of the Selection Committee [2004].
- (Test of Time Award from CGO 2005), Member of the Selection Committee [2015].

Program Committee Member

Programming Languages and Compilers

- (POPL) *ACM SIGACT/SIGPLAN Symposium on Principles of Programming Languages* [2006].
- (PLDI) *ACM SIGPLAN Conference on Programming Language Design and Implementation* [2002, 1994].
- (PPoPP) *ACM SIGPLAN Symposium on Principles and Practices of Parallel Programming* [2012].
- (PPPJ) *International Conference on the Principles and Practice of Programming on the Java Platform* [2014].

- (CGO) *IEEE/ACM International Symposium on Code Generation and Optimization* [2011, 2010, 2006, 2004, 2003].
- (CC) *International Conference on Compiler Construction* [2017, 2007, 1998, 1996, 1994].
- (ICCL) *IEEE International Conference on Computer Languages* [1998].
- (APLAS) *The ASIAN Symposium on Programming Languages and Systems* [2011, 2008].
- (ISMM) *International Symposium on Memory Management* [2019, 2011].
- (EXADAPT) *Second International Workshop on Adaptive Self-tuning Computing Systems for the Exaflop Era* [2012, 2011].
- (COCV) *International Workshop on Compiler Optimization Meets Compiler Verification* (with ETAPS) [2004, 2002].
- (PEPM) *ACM SIGPLAN Workshop on Partial Evaluation and Semantics based Program Manipulation* (with PLDI) [2003].
- (MSP) *Workshop on Memory System Performance* (with PLDI) [2002].

Computer Architecture

- (ASPLOS) *ACM International Conference on Architectural Support for Programming Languages and Operating Systems* [2018].
- (Top Picks) *IEEE Micro's Top Picks from Computer Architecture Conferences* [2007, 2005].
- (ISCA) *ACM/IEEE International Symposium on Computer Architecture* [2012, 2007].
- (HPCA) *IEEE International Symposium on High Performance Computer Architecture* [2008, 2006, 2005].
- (MICRO) *IEEE/ACM International Symposium on Microarchitecture* [2018, 2006, 2005, 2004, 2003, 2002, 2001, 2000, 1995].
- (ICS) *ACM International Conference on Supercomputing* [2004, 2003, 2001].
- (PACT) *International Conference on Parallel Architectures and Compilation Techniques* [2017, 2010, 2009, 1998, 1997, 1996, 1994].
- (ISPASS) *IEEE International Symposium on Performance Analysis of Systems and Software* [2019, 2011, 2008, 2003].
- (HiPEAC) *International Conf. on High-Performance Embedded Architectures and Compilers* [2010, 2007, 2005].
- (HPPC) *Workshop on Hardware-support for Parallel Program Correctness* [2011].
- (INTERACT) *Workshop on Interaction Between Compilers and Computer Architectures* [2012, 2011, 2010].
- (M2A2) *International Workshop on Multicore and Multithreaded Architectures and Algorithms* [2015, 2014, 2013, 2012, 2011, 2010].
- (PESPMA) *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures* (with ISCA) [2010, 2009].
- (SAMOS) *International Workshop on Systems, Architectures, Modeling, and Simulation* [2009, 2008].
- (RAAW) *Workshop on Reconfigurable and Adaptive Architectures* (with MICRO) [2007, 2006].
- (COLP) *Workshop on Compilers and Operating Systems for Low Power* (with PACT) [2003, 2002, 2001, 2000].

- (VPW) *Value Prediction Workshop* (with ISCA) [2003].
- (SSRS) *Workshop on Software Support for Reconfigurable Systems* (with HPCA) [2003].

Parallel Computing

- (IA³) *7th Workshop on Irregular Applications: Architectures and Algorithms* (with SC) [2018, 2017].
- (CCGrid) *IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing* [2015].
- (IPDPS) *IEEE International Parallel and Distributed Processing Symposium* [2014, 2013].
- (HPCC) *IEEE International Conf. on High Performance Computing and Communications* [2016, 2015].
- (ICPADS) *IEEE International Conference on Parallel and Distributed Systems* [2015, 2014, 2013, 2011].
- (HiPC) *High Performance Computing Conference* [2013].
- (PDCN) *Parallel and Distributed Computing and Networks* [2006, 2004].
- (ICPP) *International Conference on Parallel Processing* [2015, 2003].
- (PDCS) *International Conference on Parallel and Distributed Computing Systems* [2000, 1998, 1997, 1992].

Software Engineering

- (QRS) *IEEE International Conference on Software Quality, Reliability, and Security* [2018, 2017, 2016, 2015].
- (ICSME) *IEEE International Conference on Software Maintenance and Evolution* [2014].
- (ICSM) *IEEE International Conference on Software Maintenance* [2013].
- (QSIC) *International Conference on Quality Software* [2014, 2013, 2012, 2011, 2010].
- (RV) *International Conference on Runtime Verification* [2011, 2010].
- (PASTE) *ACM SIGPLAN-SIGSOFT Workshop on Program Analysis for Software Tools and Engineering* [2008, 1998].
- (WODA) *Tenth International Workshop on Dynamic Analysis* [2015, 2014, 2012].
- (REGRESSION) *The Second International Workshop on Regression Testing* [2012].
- (Compute) *ACM Compute Conference* [2008].
- (DASC) *IEEE International Conference on Dependable, Autonomic and Secure Computing* [2014].
- (ICSOFT) *International Conference on Software and Data Technologies* [2006].
- (eTX) *eclipse Technology eXchange Workshop* (with OOPSLA) [2003].

Embedded Systems

- (LCTES) *ACM SIGPLAN Conference on Languages, Compilers, and Tools for Embedded Systems* [2014, 2013, 2004].
- (LCTES/SCOPES) *ACM SIGPLAN Joint Conference on Languages, Compilers, and Tools for Embedded Systems & Software and Compilers for Embedded Systems* [2002].
- (CASES) *International Conf. on Compilers, Architectures and Synthesis for Embedded Systems* [2016, 2015, 2014, 2013, 2012, 2011, 2010, 2008, 2006, 2005, 2004, 2002, 1998].

- (SAMOS) *International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation* [2018, 2016, 2015, 2014, 2013, 2012, 2011, 2010].
- (DATE) *Design, Automation and Test in Europe* [2007].
- (SAC) *ACM Symp. on Applied Computing* [2018, 2016, 2015, 2014, 2013, 2012, 2011, 2010].
- (ICISS) *IEEE International Conference on Embedded Software and Systems* [2013, 2012, 2011, 2010, 2009].
- (RTCSA) *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications* [2013, 2010, 2009].
- (ESA) *IEEE International Symposium on Advanced Topics on Embedded Systems and Applications* [2011].
- (EUC) *International Conference on Embedded And Ubiquitous Computing* [2004].
- (FutureTech) *International Conference on Future Information Technology* [2012, 2010].
- (LCTES) *ACM SIGPLAN Workshop on Languages, Compilers, and Tools for Embedded Systems (with PLDI)* [2001, 1998].
- (LCT-RTS) *ACM SIGPLAN Workshop on Language, Compiler, and Tool Support for Real-Time Systems (with PLDI)* [1995].
- (SCOPEs) *International Workshop on Software and Compilers for Embedded Systems* [2004, 2003].
- (WESAPEC) *International Workshop on Embedded System Architectures for Pervasive Devices and Computers (with IPC)* [2007].
- (SoC) *International Workshop on SoC and MCoS design (with MoMM)* [2006].
- (EC) *International Workshop on Embedded Computing* [2006].
- (CTCES) *Workshop on Compilers and Tools for Constrained Embedded Systems (with CASES)* [2005, 2004, 2003].
- (ECS) *International Workshop on Embedded Computing Systems (with ICDCS)* [2004].
- (LARTES) *IEEE Workshop on large Scale Real-Time and Embedded Systems (with RTSS)* [2002].

External Review Committee Member

- (ISCA) *ACM/IEEE International Symposium on Computer Architecture* [2015].
- (PLDI) *ACM SIGPLAN Conference on Programming Language Design and Implementation* [2015, 2014, 2013, 2010].
- (MICRO) *Annual IEEE/ACM International Symposium on Microarchitecture* [2014, 2012].
- (ASPLOS) *ACM International Conference on Architectural Support for Programming Languages and Operating Systems* [2016, 2015, 2012].
- (POPL) *ACM SIGACT/SIGPLAN Symposium on Principles of Programming Languages* [2012].

Membership

- ACM (Fellow & Lifetime Member).
- IEEE (Fellow).
- AAAS (Fellow).
- Member – SIGPLAN, SIGSOFT, SIGARCH, and SIGMICRO.
- Associate Member – HiPEAC, <http://www.hipeac.net>.

Other Refereeing and Reviewing

- **(Proposals)** NSF Panels for Programs – XPS, Expeditions in Computing, CAREER, CCF, Compilers, Computer Architecture, and ITR; Fonds Wetenschappelijk Onderzoek - Vlaanderen, Belgium; Fonds National de la Recherche, Luxembourg; The Knowledge Foundation, Sweden; Science Foundation, Ireland; UKIERI, British Council; NSERC Canada; University Grants Council of Hong Kong; UCMEXUS Review Panel; and UC Discovery Review Panel.
- **(Journals)** ACM TOSEM, ACM TOPLAS, ACM TECS, ACM TACO, ACM TODAES, ACM LOPLAS, IEEE TPDS, IEEE TSE, IEEE TC, IEEE Computer, IEEE Software, IEEE Micro, IEEE PDT, CACM, SP&E, JPDC, IJPP, Parallel Computing, J. Supercomputing, JSTVR, and JPL.
- **(Conferences)** SIGPLAN-SIGACT POPL, SIGPLAN PLDI, IEEE/ACM MICRO, ACM ASPLOS, IEEE/ACM ISCA, IEEE HPCA, ACM ICS, IEEE ICCL, CC, PEPM, CGO, ISPASS, PACT, FDDO, LCTES, CASES, SCOPES, LCPC, COLP, ISSRE, IEEE SRDS, IEEE IPPS, ICPP, HiPC, PARLE, DMCC, PDCS, Supercomputing, ICPADS, and IEEE SPDP.
- **(Others)** PhD Dissertations – SIGPLAN Doctoral Dissertation Award Nominees; Video Lectures – University Video Communications; and Book – IEEE Computer Society.

RESEARCH GRANTS

National Science Foundation, Software and Hardware Foundations, *SHF: Small: GPU-dedicated Graph Transformations for Accelerating Iterative Graph Analytics*, CCF-1813173, \$499,987, 10/2018 – 9/2021 (PI: Z. Zhao; Co-PI: R. Gupta).

National Science Foundation, Secure & Trustworthy Cyberspace, *TWC: Small: Collaborative: Improving Android Security with Dynamic Slicing*, CNS-1617424, UCR Portion \$250,000, 9/2016 – 8/2019 (PIs: I. Neamtii - NJIT; R. Gupta - UCR).

National Science Foundation, Software and Hardware Foundations, *SHF: Small: Transformations for Synergistic Analysis of Large Evolving Graphs*, CCF-1524852, \$400,000, 7/2015 – 6/2019 (PI: R. Gupta).

Intel Corporation, *Dynamic Slicing on Android-x86*, \$65,000, 7/2014 – 9/2015 (PI: I. Neamtii; Co-PI: R. Gupta).

National Science Foundation, Software and Hardware Foundations, *SHF: Small: Memory Consistency – Hardware, Compiler, and Programming Support*, \$539,999, CCF-1318103: \$450,000 (9/2013) + CCF-1547990: \$89,999 supplement (8/2015), 9/2013 – 8/2017 (PI: R. Gupta).

Intel Corporation, *Dynamic Slicing for Interactive Debugging of Multithreaded Programs*, \$65,000, 7/2013 – 9/2014 (PI: R. Gupta; Co-PI: I. Neamtii).

Google Research Award, *Size Oblivious Programming for Large Dynamic Data Structures*, \$48,500, 03/2013 – 02/2014 (PI: R. Gupta).

National Science Foundation, Computing Systems Research, *EAGER: Developing a Programming Environment for Heterogeneous Multiprocessors*, CNS-1157377, \$299,288, 9/2012 – 8/2014 (PI: L.N. Bhuyan; Co-PI: R. Gupta).

Intel Corporation, *Supporting Dynamic Slicing for Interactive Debugging*, \$65,000, 6/2012 – 5/2013 (PI: R. Gupta).

National Science Foundation, Software and Hardware Foundations, *WORKSHOP: Support for the Sixteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2011)*, CCF-1059827, \$15,000, 12/2010 – 6/2011 (PI: P. Brisk; Co-PI: R. Gupta).

- National Science Foundation**, Software and Hardware Foundations, *SHF: Medium: Programmable Monitoring Framework for Multicore Systems*, CCF-0963996, \$726,000, 9/2010 – 8/2014 (PI: R. Gupta; Co-PI: I. Neamtiu).
- National Science Foundation**, Software and Hardware Foundations, *SHF: Medium: Hardware/Software Partitioning for Hybrid Shared Memory Multiprocessors*, CCF-0905509, \$800,000, 9/2009 – 8/2015 (PI: L. Bhuyan; Co-PIs: R. Gupta, W. Najjar).
- National Science Foundation**, Computing Systems Research, *Scalable and Efficient Dynamic Information Flow Tracking in Multithreaded Programs*, CNS-0751961/0719791, UCR funds \$180,000, 9/2007 – 8/2010 (PI: R. Gupta; Co-PI: X. Zhang).
- National Science Foundation**, Computing Research Infrastructure, *An Advanced Infrastructure for Generation, Storage, and Analysis of Program Execution Traces*, CNS-0751949/0708199, UCR funds \$85,000, 9/2007 – 9/2010 (PI: R. Gupta; Co-PIs: N. Gupta, X. Zhang).
- National Science Foundation**, Computing Systems Research, *ExPert: dynamic analysis based fault location via Execution Perturbations*, CNS-0810906/0614707, \$332,000, 9/2006 – 8/2010 (PIs: R. Gupta, N. Gupta).
- Microsoft Research**, Redmond, Washington, *Integrating Dynamic Slicing into the coredbg Debugger*, \$48,000, 4/2006 – 3/2007 (PI: N. Gupta; Co-PI: R. Gupta).
- National Science Foundation**, Computing Processes and Artifacts, *Dynamic Unmasking of Compiler Optimizations and Obfuscations*, CCF-0753470/0541382, \$300,000, 2/2006 – 1/2010 (PI: R. Gupta).
- IBM**, Eclipse Innovation Award, *An Eclipse Module for Matching Execution Histories of Program Versions*, \$27,000, 1/2005 – 12/2005 (PI: R. Gupta; Co-PI: N. Gupta).
- National Science Foundation**, ITR Medium Grants, *Morphable Software Services: Self-Modifying Programs for Distributed Embedded Systems*, CCF-0324969, U. of Arizona funds \$166,225, 10/2003 – 9/2007 (PI: K. Schwan; Co-PIs: T. Balch, G. Eisenhauer, R. Gupta, S. Pande, C. Pu, H-H. S. Lee).
- Microsoft Research**, Redmond, Washington, *Using Phoenix for Program Slicing and its Application to Defect Analysis*, \$121,000, 9/2003 – 8/2006. Matching funds from ACIST at Univ. of Arizona \$42,500 (PI: R. Gupta).
- Intel Corporation**, MRL, Santa Clara, California, *Compiling for Processors with Fine-Grained Threading, Heterogenous Cores, and Sophisticated Data Management*, \$108,500, 9/2003 – 8/2006 (PI: R. Gupta).
- IBM**, Eclipse Innovation Award, *Protecting Software through Slicing and Obfuscation Transformations*, \$27,000, 1/2003 – 12/2003 (PI: R. Gupta). Seed grant of \$14,000 provided by ACIST, Univ. of Arizona.
- National Science Foundation**, Computer Systems Architecture, *Information Encoding for Energy Efficient Processor Design*, CCF-0208756, \$280,000, 9/2002 – 8/2006 (PI: R. Gupta).
- National Science Foundation**, ITR Small Grants, *Code and Data Segment Optimizations for Mixed Width Instruction Set Embedded Processor*, CCF-0220334, U. of Arizona funds \$149,112, 9/2002 – 8/2005 (PI: R. Gupta; Co-PI: S. Pande). Seed grant of \$10,000 provided by ACIST, Univ. of Arizona.
- National Science Foundation**, Compilers, *Data Compression Techniques for Improving Memory Hierarchy Performance*, CCF-0105355, \$270,000, 9/2001 – 8/2005 (PI: R. Gupta).
- DARPA**, Power Aware Computing/Communication, *Power-Adaptive Microarchitecture and Compiler Design for Mobile Computing*, Award no. F29601-00-1-0183, \$572,396, 7/2000 – 11/2002 (PI: R. Gupta; Co-PIs: S. Onder and S. Pande).

National Science Foundation, CISE Research Infrastructure, *Optimization of Distributed and Networked Systems: A Spectrum of Techniques*, EIA-0080123, \$1,396,252, 9/2000 – 9/2005 (PIs: G.R. Andrews, S. Debray, R. Gupta, S. Pink, and R.T. Snodgrass).

Intel Corporation, MRL, Santa Clara, California, *Exploiting Speculation and Predication for Branch and Load Optimizations*, \$96,000, 9/1999 – 6/2002 (PI: R. Gupta).

National Science Foundation, Experimental Systems, *Experimental Evaluation of Scalable Optimization Techniques*, EIA-9806525, \$400,000, 9/1998 – 9/2001 (PI: M.L. Soffa; Co-PIs: R. Gupta, L.L. Pollock, and D. Whalley).

National Science Foundation, Compilers, *A Framework for Path and Resource Sensitive Optimizations*, CCR-0096122/CCR-9808590, \$360,000, 9/1998 – 9/2002 (PI: R. Gupta; Co-PI: M.L. Soffa).

Intel Corporation, MRL, Santa Clara, California, *Machine Dependent Analysis for Exploiting ILP in VLIW Architectures*, \$32,000, 1/1998 – 12/1998 (PI: R. Gupta).

Hewlett Packard Laboratories, Chelmsford, Massachusetts, *Comparative Debugging of Optimized Code*, \$236,131, 5/1997 – 4/1998 (PI: M.L. Soffa; Co-PI: R. Gupta).

Hewlett Packard Laboratories, Palo Alto, California, *Optimizations Techniques for Superscalar and VLIW Architectures*, \$34,484, 5/1997 – 4/1998 (PI: R. Gupta; Co-PI: M.L. Soffa).

National Science Foundation, Operating Systems, *On-line Avoidance of Monitoring Intrusion in Distributed Systems*, CCR-9996362/CCR-9704350, \$156,012, 6/1997 – 8/2000 (PI: R. Gupta).

Intel Corporation, Santa Clara, California, *Machine Dependent Analysis for Exploiting ILP in VLIW Architectures*, \$72,038, 1/1997 – 12/1997 (PI: R. Gupta).

National Science Foundation, Compilers, *Research Experience with Undergraduates*, supplement to *Loop Transformations and Scheduling Strategies for Parallelizing Software*, CCR-9157371, \$4,950, 8/1996 – 7/1997 (PI: R. Gupta).

Hewlett Packard Laboratories, Palo Alto, California, *Optimizations Techniques for Superscalar/VLIW Architectures*, \$68,550, 1/1996 – 4/1997 (PI: R. Gupta; Co-PI: M.L. Soffa).

Hewlett Packard Laboratories, Chelmsford, Massachusetts, *Debugging of Optimized Code*, \$102,290, 1/1996 – 4/1997 (PI: M.L. Soffa; Co-PI: R. Gupta).

Intel Corporation, Santa Clara, California, *Static Analysis and Optimization Techniques for Exploiting ILP in Superscalar/VLIW Architectures*, \$20,000, 1/1996 – 12/1996 (PI: R. Gupta).

National Science Foundation, Software Engineering, *Demand Driven Computation of Partial Data Flow and its Application in Software Engineering*, CCR-9402226, \$240,000, 9/1995 – 8/1998 (PI: M.L. Soffa; Co-PI: R. Gupta).

Hewlett Packard Laboratories, Palo Alto, California, *Data Flow Analysis and Optimization Techniques for Superscalar/VLIW Architectures*, \$57,022, 3/1995 – 4/1996 (PI: R. Gupta).

Intel Corporation, Santa Clara, California, *Optimizations to Facilitate ILP for Superscalar/VLIW Architectures*, \$21,116, 1/1995 – 12/1995 (PI: R. Gupta).

Digital Equipment Corporation, Pittsburgh, Pennsylvania, *Equipment Support for Studying the Interaction between Transformations and Scheduling Strategies in Compilers*, \$14,661, 2/1993 (PI: R. Gupta).

Siemens Corporate Research, Inc., Princeton, New Jersey, *Research Assistantships*, \$25,000, 6/1992 (PI: R. Gupta).

Honeywell Inc., Minneapolis, Minnesota, *PORTAL Compiler and Fine-Grained Adaptation of Real-Time Schedules*, \$5,000, 4/1992 – 8/1992 (PI: R. Gupta).

Philips Laboratories, Briarcliff Manor, New York, *POOMA Multiprocessor Prototype*, \$35,000, 8/1992 (PI: R. Gupta).

National Science Foundation, Compilers, *Loop Transformations and Scheduling Strategies for Parallelizing Software*, Presidential Young Investigator Award CCR-9157371, \$271,109, 8/1991 – 12/1997 (PI: R. Gupta).

PATENTS ISSUED

1. **US Patent 8,321,840**: *Software Flow Tracking Using Multiple Threads*, Nov. 2012. *Inventors*: V. Nagarajan, H-S. Kim, Y. Wu, and R. Gupta. *Assignee*: Intel Corporation.
2. **US Patent 6,848,100**: *Hierarchical Software Path Profiling*, Jan. 2005. *Inventors*: Y. Wu, A. Adl-Tabatabai, D. Berson, J.Z. Fang, and R. Gupta. *Assignee*: Intel Corporation.
3. **US Patent 6,044,221**: *Optimizing Code Based On Resource Sensitive Hoisting and Sinking*, March 2000. *Inventors*: R. Gupta, D. Berson, and J.Z. Fang. *Assignee*: Intel Corporation.
4. **US Patent 5,999,736**: *Optimizing Code by Exploiting Speculation and Predication with a Cost-Benefit Data Flow Analysis Based on Path Profiling Information*, December 1999. *Inventors*: R. Gupta, D. Berson, and J.Z. Fang. *Assignee*: Intel Corporation.
5. **US Patent 5,802,374**: *Synchronizing Parallel Processors using Barriers Extending Over Specific Multiple-Instruction Regions in Each Instruction Stream*, September 1998. *Inventors*: R. Gupta and M. Epstein. *Assignee*: Philips Electronics.
6. **US Patent 5,787,272**: *Method and Apparatus for Improving Synchronization Time in a Parallel Processing System*, July 1998. *Inventors*: R. Gupta and M. Epstein. *Assignee*: Philips Electronics.
7. **US Patent 5,317,734**: *Method of Synchronizing Parallel Processors Employing Channels and Compiling Method Minimizing Cross-Processor Data Dependencies*, May 1994. *Inventor*: R. Gupta. *Assignee*: Philips Electronics.
8. **US Patent 5,303,377**: *Method for Compiling Computer Instructions for Increasing Instruction Cache Efficiency*, April 1994. *Inventors*: R. Gupta and C-H. Chi. *Assignee*: Philips Electronics.
9. **US Patent 5,127,092**: *Apparatus and Method for Collective Branching in a Multiple Instruction Stream Multiprocessor where any of the Parallel Processors is Scheduled to Evaluate the Branching Condition*, June 1992. *Inventors*: R. Gupta and M. Epstein. *Assignee*: Philips Electronics.

JOURNAL PUBLICATIONS

1. Z. Benavides, K. Vora, R. Gupta, and X. Zhang, "Annotation Guided Collection of Context-Sensitive Parallel Execution Profiles," *Springer's Formal Methods in System Design (FMSD)*, special issue of extended versions of selected papers from RV 2017, 28 pages, 2018 (final decision pending following minor revision).
2. S-C. Koduru, K. Vora, and R. Gupta, "Software Speculation on Caching DSMs," *International Journal of Parallel Programming (IJPP)*, Vol. 46, Issue 2, pages 313-332, April 2018.
3. K. Vora, R. Gupta, and G. Xu, "Synergistic Analysis of Evolving Graphs," *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 13, Issue 4, Article No. 32, 27 pages, December 2016.

4. K.K. Pusukuri, R. Gupta, and L.N. Bhuyan, "Tumbler: An Effective Load Balancing Technique for MultiCPU Multicore Systems," *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 12, Issue 4, Article No. 36, 24 pages, January 2016.
5. K.K. Pusukuri, R. Gupta, and L.N. Bhuyan, "ADAPT: A Framework for Co-Scheduling Multi-threaded Programs," *ACM Transactions on Architecture and Code Optimization (TACO)*, special issue of papers presented at HiPEAC 2013, Volume 9, Issue 4, Article No. 45, 25 pages, January 2013.
6. M.E. Belviranli, L.N. Bhuyan, and R. Gupta, "A Dynamic Self Scheduling Scheme for Heterogeneous Multiprocessor Architectures," *ACM Transactions on Architecture and Code Optimization (TACO)*, special issue of papers presented at HiPEAC 2013, Volume 9, Issue 4, Article No. 57, 20 pages, January 2013.
7. V. Nagarajan, D. Jeffrey, and R. Gupta, "A System for Debugging via Online Tracing and Dynamic Slicing," *Software – Practice And Experience (SP&E)*, Vol. 42, No. 8, pages 995-1014, August 2012.
8. M. Feng, C. Lin, and R. Gupta, "PLDS: Partitioning Linked Data Structures for Parallelism," *ACM Transactions on Architecture and Code Optimization (TACO)*, special issue of papers presented at HiPEAC 2012, Volume 8, Issue 4, Article No. 38, 21 pages, January 2012.
9. K.K. Pusukuri, R. Gupta, and L.N. Bhuyan, "Thread Tranquilizer: Dynamically Reducing Performance Variation," *ACM Transactions on Architecture and Code Optimization (TACO)*, special issue of papers presented at HiPEAC 2012, Volume 8, Issue 4, Article No. 46, 21 pages, January 2012.
10. C. Lin V. Nagarajan, and R. Gupta, "Efficient Sequential Consistency Using Conditional Fences," *International Journal of Parallel Programming (IJPP)*, Vol. 40, No. 1, pages 84-117, special issue of Best Papers from PACT 2010, Feb. 2012.
11. M. Feng, C. Tian, C. Lin, and R. Gupta, "Dynamic Access Distance Driven Cache Replacement," *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 8, Issue 3, Article No. 14, 30 pages, October 2011.
12. D. Jeffrey, Y. Wang, C. Tian, and R. Gupta, "Isolating Bugs in Multithreaded Programs Using Execution Suppression," *Software – Practice And Experience (SP&E)*, Vol. 41, No. 11, pages 1259-1288, October 2011.
13. D. Jeffrey, V. Nagarajan, and R. Gupta, "Execution Suppression: An Automated Iterative Technique for Locating Memory Bugs," *ACM Transactions on Programming Languages and Systems (TOPLAS)*, Volume 32, Issue 5, Article No. 17, 36 pages, May 2010.
14. C. Tian, M. Feng, V. Nagarajan, and R. Gupta, "Speculative Parallelization of Sequential Loops On Multicores," *International Journal of Parallel Programming (IJPP)*, Vol. 37, No. 5, pages 508-535, October 2009.
15. C. Tian, V. Nagarajan, R. Gupta, and S. Tallam, "Automated Dynamic Detection of Busy-Wait Synchronizations," *Software – Practice And Experience (SP&E)*, Vol. 39, No. 11, pages 947-972, Aug. 2009.
16. V. Nagarajan, R. Gupta, and A. Krishnaswamy, "Compiler-Assisted Memory Encryption for Embedded Processors," *Transactions on High Performance Embedded Architectures and Compilers (THiPEAC)*, special issue of Best Papers from HiPEAC 2007, LNCS 5470, Springer, Vol. 2, pages 23-44, 2009.
17. V. Nagarajan and R. Gupta, "Runtime Monitoring on Multicores via OASES," *ACM SIGOPS Operating Systems Review*, special issue on the interaction among the OS, Compilers, and Multicore Processors, pages 15-24, Vol. 43, No. 2, April 2009 (invited paper).

18. S. Tallam and R. Gupta, "Unified Control Flow and Dependence Traces," *ACM Transactions on Architecture and Code Optimization* (ACM TACO), Vol. 4, No. 3, 31 pages, September 2007.
19. X. Zhang, N. Gupta, and R. Gupta, "Locating Faulty Code by Multiple Points Slicing," *Software - Practice & Experience* (SP&E), Vol. 37, Issue 9, pages 935-961, July 2007.
20. X. Zhang, N. Gupta, and R. Gupta, "A Study of Effectiveness of Dynamic Slicing in Locating Real Faults," *Empirical Software Engineering Journal*, Vol. 12, No. 2, pages 143-160, April 2007.
21. Y. Lin, Y. Zhang, and R. Gupta, "The Design and Evaluation of Path Matching Schemes on Compressed Control Flow Traces," *Journal of Systems and Software*, Vol. 80, No. 3, pages 396-409, 2007.
22. Y. Zhang and R. Gupta, "Compressing Heap Data for Improved Memory Performance," *Software - Practice & Experience* (SP&E), Volume 36, Issue 10, pages 1081-1111, August 2006.
23. X. Zhang and R. Gupta, "Whole Execution Traces and their Applications," *ACM Transactions on Architecture and Code Optimization* (ACM TACO), Vol. 2, No. 3, pages 301-334, September 2005.
24. X. Zhang, R. Gupta, and Y. Zhang, "Cost and Precision Tradeoffs of Dynamic Slicing Algorithms," *ACM Transactions on Programming Languages and Systems* (ACM TOPLAS), Vol. 27, No. 4, pages 631-661, July 2005.
25. A. Krishnaswamy and R. Gupta, "Dynamic Coalescing of 16-bit Instructions," *ACM Transactions on Embedded Computing Systems* (ACM TECS), in special issue of selected LCTES'03 papers, Vol. 4, No. 1, pages 3-37, February 2005.
26. J. Yang, R. Gupta, and C. Zhang, "Frequent Value Encoding for Low Power Data Buses," *ACM Transactions on Design Automation of Electronic Systems* (ACM TODAES), Vol. 9, No. 3, pages 354-384, July 2004.
27. A. Krishnaswamy and R. Gupta, "Mixed Width Instruction Sets," *Communications of the ACM* (CACM), in special section on Program Compaction, Vol. 46, No. 8, pages 47-52, August 2003.
28. X. Yuan, R. Melhem, and R. Gupta, "Algorithms for Supporting Compiled Communication," *IEEE Transactions on Parallel and Distributed Systems* (IEEE TPDS), Vol. 14, No. 2, pages 107-118, February 2003.
29. J. Yang and R. Gupta, "Frequent Value Locality and its Applications," *ACM Transactions on Embedded Computing Systems* (ACM TECS), special inaugural issue on memory systems, Vol. 1, No. 1, pages 79-105, November 2002.
30. S. Onder and R. Gupta, "Dynamic Memory Disambiguation in Presence of Out-of-order Store Issuing," *The Journal of Instruction Level Parallelism* (IJPP), <http://www.jilp.org/vol4>, Vol. 4, 2002.
31. X. Yuan, R. Melhem, and R. Gupta, "Performance of Multi-Hop Communications Using Logical Topologies on Optical Torus Networks," *Journal of Parallel and Distributed Computing* (JPDC), Vol. 61, No. 6, pages 748-766, June 2001.
32. R. Gupta, S. Pande, K. Psarris, and V. Sarkar, "Compiling for Parallel Systems," *Parallel Computing journal*, North Holland, Vol. 25, No. 13-14, pages 1741-1783, December 1999 (invited paper).
33. X. Yuan, R. Melhem, and R. Gupta, "Distributed Path Reservation Algorithms for Multiplexed All-Optical Interconnection Networks," *IEEE Transactions on Computers* (IEEE TC), Vol. 48, No. 12, pages 1355-1363, December 1999.

34. X. Yuan, R. Melhem, R. Gupta, Y. Mei, and C. Qiao, "Distributed Control for Wavelength Reservation and their Performance Evaluation," *Photonic Network Communications* journal, Kluwer Academic Publishers, Vol. 1, No. 3, pages 207-218, November 1999.
35. C. Gong, R. Melhem, and R. Gupta, "On-Line Error Detection through Data Duplication in Distributed-Memory Systems," *Microprocessor and Microsystems*, a special issue on Fault Tolerance, Vol. 21, No. 3, pages 197-209, December 1997.
36. X. Yuan, R. Gupta, and R. Melhem, "Demand-Driven Data Flow Analysis for Communication Optimization," *Parallel Processing Letters*, Vol. 7, No. 4, pages 359-370, December 1997.
37. E. Duesterwald, R. Gupta, and M.L. Soffa, "A Practical Framework for Demand-Driven Interprocedural Data Flow Analysis," *ACM Transactions on Programming Languages and Systems* (ACM TOPLAS), Vol. 19, No. 6, pages 992-1030, November 1997.
38. R. Gupta, M.L. Soffa, and J.H. Howard, "Hybrid Slicing: Integrating Dynamic Information with Static Analysis," *ACM Transactions on Software Engineering and Methodology* (ACM TOSEM), Vol. 6, No. 4, pages 370-397, October 1997.
39. C. Gong, R. Melhem, and R. Gupta, "Loop Transformations for Fault Detection on Massively Parallel Systems," *IEEE Transactions on Parallel and Distributed Systems* (IEEE TPDS), Vol. 7, No. 12, pages 1239-1250, December 1996.
40. R. Bodik and R. Gupta, "Array Data-Flow Analysis for Load-Store Optimizations in Superscalar Architectures," *International Journal of Parallel Programming* (IJPP), special issue on Languages and Compilers for Parallel Computing, Vol. 24, No. 6, pages 481-512, 1996.
41. R. Gupta, M.J. Harrold, and M.L. Soffa, "Program Slicing-Based Regression Testing Techniques," *Journal of Software Testing, Verification and Reliability*, Vol. 6, No. 2, pages 83-112, June 1996.
42. R. Gupta and M. Spezialetti, "A Compact Task Graph Representation for Real-Time Scheduling," *Real Time Systems* journal, Vol. 11, No. 1, pages 71-102, 1996.
43. M. Spezialetti and R. Gupta, "Loop Monotonic Statements," *IEEE Transactions on Software Engineering* (IEEE TSE), Vol. 21, No. 6, pages 497-505, June 1995.
44. R. Gupta, "Generalized Dominators," *Information Processing Letters*, Vol. 53, pages 193-200, 1995.
45. R. Kramer, R. Gupta, and M.L. Soffa, "The Combining DAG: A Technique for Parallel Data Flow Analysis," *IEEE Transactions on Parallel and Distributed Systems* (IEEE TPDS), Vol. 5, No. 8, pages 805-813, August 1994.
46. R. Gupta, M.L. Soffa, and D. Ombres, "Efficient Register Allocation Via Coloring using Clique Separators," *ACM Transactions on Programming Languages and Systems* (ACM TOPLAS), Vol. 16, No. 3, pages 370-386, May 1994.
47. R. Gupta, "Optimizing Array Bound Checks using Flow Analysis," *ACM Letters on Programming Languages and Systems* (ACM LOPLAS), Vol. 2, Nos. 1-4, pages 135-150, March-December 1994.
48. R. Gupta and M.L. Soffa, "Employing Static information in the Generation of Test Cases," *Journal of Software Testing, Verification and Reliability*, Vol. 3, No. 1, pages 29-48, December 1993.
49. M.J. Harrold, R. Gupta, and M.L. Soffa, "A Methodology for Controlling the Size of a Test Suite," *ACM Transactions on Software Engineering and Methodology* (ACM TOSEM), Vol. 2, No. 3, pages 270-285, July 1993.

50. R. Gupta, "SPMD Execution of Programs with Pointer-based Data Structures on Distributed-Memory Machines," *Journal of Parallel and Distributed Computing* (JPDC), special issue on Multicomputer Programming and Application, Vol. 16, No. 2, pages 92-107, October 1992.
51. P. Gopinath, T. Bihari, and R. Gupta, "Compiler Techniques for Generating Predictable Object-Oriented Real-Time Software," *IEEE Software*, special issue on Real-time systems, pages 45-50, September 1992.
52. R. Gupta, "Synchronization and Communication Costs of Loop Partitioning on Shared-Memory Multiprocessor Systems," *IEEE Transactions on Parallel and Distributed Systems* (IEEE TPDS), Vol. 3, No. 4, pages 505-512, July 1992.
53. R. Gupta and S. Lee, "Exploiting Parallelism on a Fine-Grained MIMD Architecture Based Upon Channel Queues," *International Journal of Parallel Programming* (IJPP), Vol. 21, No. 5, pages 169-192, June 1992.
54. R. Gupta and M.L. Soffa, "Compile-time Techniques for Improving Scalar Access Performance in Parallel Memories," *IEEE Transactions on Parallel and Distributed Systems* (IEEE TPDS), Vol. 2, No. 2, pages 138-148, April 1991.
55. R. Gupta and M. Epstein, "Achieving Low Cost Synchronization in a Multiprocessor System," *Future Generation Computer Systems Journal*, special issue of selected papers from PARLE'89 Conference, Vol. 6, No. 3, pages 255-269, December 1990.
56. R. Gupta and M. Epstein, "High Speed Synchronization of Processors Using Fuzzy Barriers," *International Journal of Parallel Programming* (IJPP), Vol. 19, No. 1, pages 53-73, 1990.
57. R. Gupta, "Debugging Code Reorganized by a Trace Scheduling Compiler," *Structured Programming*, Vol. 11, No. 3, pages 141-150, July 1990.
58. R. Gupta and M.L. Soffa, "Region Scheduling: An Approach for Detecting and Redistributing Parallelism," *IEEE Transactions on Software Engineering* (IEEE TSE), Vol. 16, No. 4, pages 421-431, April 1990.
59. R. Gupta and M.L. Soffa, "Compilation Techniques for a Reconfigurable LIW Architecture," *The Journal of Supercomputing*, Vol. 3, pages 271-304, 1989.
60. T.S. Anand and R. Gupta, "A Tool for Evaluating Compiler-based Parallelization Strategies," *Transactions of IMACS, Mathematics and Computing in Simulation*, special issue on Expert Systems for Numerical Computing, Vol. 31, No. 4, pages 509-516, October 1989.
61. R. Gupta and C.R. Hill, "A Scalable Implementation of Barrier Synchronization Using an Adaptive Combining Tree," *International Journal of Parallel Programming* (IJPP), Vol. 18, No. 3, pages 161-180, June 1989.

CONFERENCE PUBLICATIONS

62. C. Xu, K. Vora, and R. Gupta, "PnP: Pruning and Prediction for Point-To-Point Iterative Graph Analytics," *ACM International Conference on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), 13 pages, Providence, RI, April 2019.
63. W-C. Lee, Y. Liu, P. Liu, S. Ma, H.J. Choi, X. Zhang, and R. Gupta, "White-Box Program Tuning," *IEEE/ACM International Symposium on Code Generation and Optimization* (CGO), 10 pages, Washington DC, Feb. 2019.
64. G. Kaur, K. Vora, S.C. Koduru, and R. Gupta, "OMR: Out-of-Core MapReduce for Large Data Sets," *ACM SIGPLAN International Symposium on Memory Management* (ISMM), pages 71-83, Philadelphia, Pennsylvania, June 2018.

65. I. Gasparis, A. Aqil, Z. Qian, C. Song, S.V. Krishnamurthy, R. Gupta, and E. Colbert, "Droid M+: Developer Support for Imbibing Android's New Permission Model," *ACM Asia Conference on Computer and Communications Security (ASIACCS)*, pages 765-776, Songdo, Incheon, Korea, June 2018.
66. H. Li, S. Li, Z. Benavides, Z. Chen, and R. Gupta, "COMPI: Concolic Testing for MPI Applications," *32nd IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 865-874, Vancouver, British Columbia, Canada, May 2016.
67. H. Li, Z. Chen, and R. Gupta, "ParaStack: Efficient Hang Detection for MPI Programs at Large Scale," *ACM/IEEE International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, Article No. 63, 12 pages, Denver, Colorado, November 2017.
68. Z. Benavides, R. Gupta, and X. Zhang, "Annotation Guided Collection of Context-Sensitive Parallel Execution Profiles," *The 17th International Conference on Runtime Verification (RV)*, LNCS, volume 10548, Springer, pages 103-120, Seattle, Washington, September 2017.
69. K. Vora, R. Gupta, and G. Xu, "KickStarter: Fast and Accurate Computations on Streaming Graphs via Trimmed Approximations," *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 237-251, Xi'an, China, April 2017.
70. K. Vora, C. Tian, R. Gupta, and Z. Hu, "CoRAL: Confined Recovery in Distributed Asynchronous Graph Processing," *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 223-236, Xi'an, China, April 2017.
71. A. Alavi, A. Quach, H. Zhang, B. Marsh, F. Ul Haq, Z. Qian, L. Lu, and R. Gupta, "Where is the Weakest Link? A Study on Security Discrepancies between Android Apps and Their Website Counterparts," *The Passive and Active Measurement Conference (PAM)*, LNCS, volume 10176, pages 100-112, Springer, Sydney, Australia, March 2017.
72. V. Singh, I. Neamtiu, and R. Gupta, "Proving Concurrent Data Structures Linearizable," *The 26th IEEE International Symposium on Software Reliability Engineering (ISSRE)*, 11 pages, Ottawa, Canada, October 2016.
73. K. Vora, G. Xu, and R. Gupta, "Load the Edges You Need: A Generic I/O Optimization for Distributive Disk-based Graph Algorithms," *USENIX Annual Technical Conference (ATC)*, pages 507-522, Denver, Colorado, June 2016.
74. A. Kusum, K. Vora, R. Gupta, and I. Neamtiu, "Efficient Processing of Large Graphs via Input Reduction," *25th ACM International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, pages 245-257, Kyoto, Japan, May-June 2016.
75. Z. Benavides, R. Gupta, and X. Zhang, "Parallel Execution Profiles," *25th ACM International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, pages 215-218, Kyoto, Japan, May-June 2016.
76. M.E. Belviranli, F. Khorasani, L.N. Bhuyan, and R. Gupta, "CuMAS: Data Transfer Aware Multi-Application Scheduling for Shared GPUs," *ACM 30th International Conference on Supercomputing (ICS)*, 12 pages, Istanbul, Turkey, June 2016.
77. F. Khorasani, B.D. Rowe II, R. Gupta, and L.N. Bhuyan, "Eliminating Intra-warp Load Imbalance in Irregular Nested Patterns via Collaborative Task Engagement," *30th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 524-533, Chicago, Illinois, May 2016.
78. V. Singh, R. Gupta, and I. Neamtiu, "Automatic Fault Location for Data Structures," *25th International Conference on Compiler Construction (CC)*, pages 99-109, Barcelona, Spain, March 2016.

79. A. Kusum, I. Neamtii, and R. Gupta, "Safe and Flexible Adaptation Via Alternate Data Structure Representations," *25th International Conference on Compiler Construction (CC)*, pages 34-44, Barcelona, Spain, March 2016.
80. F. Khorasani, R. Gupta, and L.N. Bhuyan, "Efficient Warp Execution in Presence of Divergence with Collaborative Context Collection," *The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pages 204-215, Waikiki, Hawaii, December 2015.
81. B. Zhou, I. Neamtii, and R. Gupta, "Experience Report: How Do Bug Characteristics Differ Across Severity Classes: A Multi-platform Study," *The 26th IEEE International Symposium on Software Reliability Engineering (ISSRE)*, pages 507-517, Gaithersburg, Maryland, Nov. 2015.
82. W-C. Lee, T. Bao, Y. Zheng, X. Zhang, K. Vora, and R. Gupta, "RAIVE: Runtime Assessment of Floating-Point Instability by Vectorization," *ACM SIGPLAN International Conference on Object Oriented Programming Systems, Languages and Applications (OOPSLA)*, pages 623-638, Pittsburgh, PA, October 2015.
83. F. Khorasani, R. Gupta, and L.N. Bhuyan, "Scalable SIMD-Efficient Graph Processing on GPUs," *The 24rd International Conference on Parallel Architectures and Compilation (PACT)*, pages 39-50, San Francisco, California, October 2015. Download: <https://github.com/farkhor/WS-VR/>
84. F. Khorasani, M. Belviranli, R. Gupta, and L.N. Bhuyan, "Stadium Hashing: Scalable and Flexible Hashing on GPUs," *The 24rd International Conference on Parallel Architectures and Compilation (PACT)*, pages 63-74, San Francisco, California, October 2015.
85. S-C. Koduru, K. Vora, and R. Gupta, "Optimizing Caching DSM for Distributed Software Speculation," *IEEE International Conference on Cluster Computing (CLUSTER)*, pages 452-455, Chicago, Illinois, Sept. 2015.
86. M. Belviranli, P. Deng, L.N. Bhuyan, R. Gupta, and Q. Zhu, "PeerWave: Exploiting Wavefront Parallelism on GPUs with Peer-SM Synchronization," *ACM 29th International Conference on Supercomputing (ICS)*, pages 25-35, Newport Beach, CA, June 2015.
87. B. Zhou, I. Neamtii, and R. Gupta, "A Cross-platform Analysis of Bugs and Bug-fixing in Open Source Projects: Desktop vs. Android vs. iOS," *19th International Conference on Evaluation and Assessment in Software Engineering (EASE)*, Article 7, 10 pages, Nanjing, China, April 2015.
88. B. Zhou, I. Neamtii, and R. Gupta, "Predicting Concurrency Bugs: How Many, What Kind and Where Are They?," *19th International Conference on Evaluation and Assessment in Software Engineering (EASE)*, Article 6, 10 pages, Nanjing, China, April 2015.
89. V. Singh, R. Gupta, and I. Neamtii, "MG++: Memory Graphs for Analyzing Dynamic Data Structures," *22nd IEEE International Conference on Software Analysis, Evolution, and Reengineering (SANER)*, pages 291-300, Montreal, Canada, March 2015.
90. C. Lin, V. Nagarajan, and R. Gupta, "Fence Scoping," *ACM/IEEE International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, pages 105-116, New Orleans, Louisiana, November 2014.
91. K. Vora, S-C. Koduru, and R. Gupta, "ASPIRE: Exploiting **A**synchronous **P**arallelism in **I**terative Algorithms using a **R**elaxed Consistency based DSM," *ACM SIGPLAN International Conference on Object Oriented Programming Systems, Languages and Applications (OOPSLA)*, pages 461-478, Portland, Oregon, October 2014.
92. K.K. Pusukuri, R. Gupta, and L.N. Bhuyan, "Shuffling: A Framework for Lock Contention Aware Thread Scheduling for Multicore Multiprocessor Systems," *The 23rd International Conference on Parallel Architectures and Compilation (PACT)*, pages 289-300, Edmonton, Alberta, Canada, August 2014.

93. F. Khorasani, K. Vora, R. Gupta, and L.N. Bhuyan, "CuSha: Vertex-Centric Graph Processing on GPUs," *23rd ACM International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, pages 239-251, Vancouver, Canada, June 2014. Download: <https://github.com/farkhor/CuSha/>
94. Y. Wang, H. Patil, C. Pereira, G. Lueck, R. Gupta, and I. Neamtiu, "DrDebug: Deterministic Replay based Cyclic Debugging with Dynamic Slicing," *IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pages 98-108, Orlando, Florida, February 2014. Download: <https://software.intel.com/en-us/articles/pintool-drdebug>
95. Y. Wang, R. Gupta, and I. Neamtiu, "Relevant Inputs Analysis and its Applications," *The 24th IEEE International Symposium on Software Reliability Engineering (ISSRE)*, pages 268-277, Pasadena, CA, November 2013.
96. S-C. Koduru, M. Feng, and R. Gupta, "Programming Large Dynamic Data Structures on DSM Clusters of Multicores," *7th International Conference on PGAS Programming Models (PGAS)*, pages 126-141, Edinburgh, Scotland, October 2013.
97. Y. Wang, M. Feng, R. Gupta, and I. Neamtiu, "A State-Alteration and Inspection-based Interactive Debugger," *13th International Working Conference on Source Code Analysis and Manipulation (SCAM)*, pages 84-93, Eindhoven, Netherlands, September 2013.
98. Y. Wang, I. Neamtiu, and R. Gupta, "Generating Sound and Effective Memory Debuggers," *ACM SIGPLAN International Symposium on Memory Management (ISMM)*, pages 51-62, Seattle, Washington, June 2013.
99. C. Lin, V. Nagarajan, and R. Gupta, "Address-aware Fences," *ACM 27th International Conference on Supercomputing (ICS)*, pages 313-324, Eugene, Oregon, June 2013.
100. L. Tan, M. Feng, and R. Gupta, "Lightweight Fault Detection in Parallelized Programs," *IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pages 1-11, Shenzhen, China, February 2013.
101. M. Feng, R. Gupta, and I. Neamtiu, "Effective Parallelization of Loops in the Presence of I/O Operations," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 487-498, Beijing, China, June 2012.
102. C. Lin, V. Nagarajan, R. Gupta, and B. Rajaram, "Efficient Sequential Consistency via Conflict Ordering," *ACM 17th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 273-286, London, UK, March 2012.
103. K.K. Pusukuri, R. Gupta, and L.N. Bhuyan, "Thread Reinforcer: Dynamically Determining Number of Threads via OS Level Monitoring," *IEEE International Symposium on Workload Characterization (IISWC)*, pages 116-125, Austin, Texas, November 2011.
104. K.K. Pusukuri, R. Gupta, and L.N. Bhuyan, "No More Backstabbing... A Faithful Scheduling Policy for Multithreaded Programs," *The 20th International Conference on Parallel Architectures and Compilation (PACT)*, pages 12-21, Galveston Island, Texas, October 2011.
105. M. Feng, R. Gupta, and Y. Hu, "SpiceC: Scalable Parallelism via implicit copying and explicit Commit," *16th ACM SIGPLAN Symposium on Principles and Practices of Parallel Programming (PPoPP)*, pages 69-80, San Antonio, Texas, February 2011.
106. C. Tian, C. Lin, M. Feng, and R. Gupta, "Enhanced Speculative Parallelization Via Incremental Recovery," *16th ACM SIGPLAN Symposium on Principles and Practices of Parallel Programming (PPoPP)*, pages 189-200, San Antonio, Texas, February 2011.
107. C. Lin, V. Nagarajan, and R. Gupta, "Efficient Sequential Consistency Using Conditional Fences," *The 19th International Conference on Parallel Architectures and Compilation (PACT)*, pages 295-306, Vienna, Austria, September 2010. **Recipient of a Best Paper Award.**

108. C. Tian, M. Feng, and R. Gupta, "Supporting Speculative Parallelization in the Presence of Dynamic Data Structures," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 62-73, Toronto, Canada, June 2010.
109. C. Tian, M. Feng, and R. Gupta, "Profile-Guided Parallelization Using Multiple Value Predictions," *Ninth International Symposium on Memory Management (ISMM)*, pages 63-72, Toronto, Canada, June 2010.
110. M. Feng and R. Gupta, "Detecting Virus Mutations Via Dynamic Matching," *IEEE 25th International Conference on Software Maintenance (ICSM)*, pages 105-114, Edmonton, Canada, September 2009.
111. D. Jeffrey, N. Gupta, and R. Gupta, "Effective and Efficient Localization of Multiple Faults Using Value Replacement," *IEEE 25th International Conference on Software Maintenance (ICSM)*, pages 221-230, Edmonton, Canada, September 2009.
112. V. Nagarajan, D. Jeffrey, and R. Gupta "Self-Recovery in Server Programs," *Eight International Symposium on Memory Management (ISMM)*, pages 49-58, Dublin, Ireland, June 2009.
113. V. Nagarajan and R. Gupta, "ECMon: Exposing Cache Events for Monitoring," *ACM/IEEE 36th International Symposium on Computer Architecture (ISCA)*, pages 349-360, Austin, Texas, June 2009.
114. D. Jeffrey, M. Feng, N. Gupta, and R. Gupta, "BugFix: A Learning-Based Tool to Assist Developers in Fixing Bugs," *IEEE 17th International Conference on Program Comprehension (ICPC)*, pages 70-79, Vancouver, Canada, May 2009.
115. V. Nagarajan and R. Gupta, "Architectural Support for Shadow Memory in Multiprocessors," *ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments (VEE)*, pages 1-10, Washington DC, to appear March 2009.
116. C. Tian, M. Feng, V. Nagarajan, and R. Gupta, "Copy Or Discard Execution Model For Speculative Parallelization On Multicores," *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pages 330-341, Lake Como, Italy, November 2008.
117. D. Jeffrey, N. Gupta, and R. Gupta "Identifying the Root Causes of Memory Bugs Using Corrupted Memory Location Suppression," *International Conference on Software Maintenance (ICSM)*, pages 356-365, Beijing, China, September 2008.
118. S. Tallam, C. Tian, and R. Gupta "Dynamic Slicing of Multithreaded Programs for Race Detection," *International Conference on Software Maintenance (ICSM)*, pages 97-106, Beijing, China., September 2008.
119. S. Tallam, C. Tian, R. Gupta, and X. Zhang, "Avoiding Program Failures Through Safe Execution Perturbations," *IEEE Computer Software and Applications Conference (COMPSAC)*, pages 152-159, Turku, Finland, August 2008.
120. C. Tian, V. Nagarajan, R. Gupta, and S. Tallam "Dynamic Recognition of Synchronization Operations for Improved Data Race Detection," *International Symposium on Software Testing and Analysis (ISSTA)*, pages 143-154, Seattle, July 2008.
121. D. Jeffrey, N. Gupta, and R. Gupta "Fault Localization Using Value Replacement," *International Symposium on Software Testing and Analysis (ISSTA)*, pages 167-178, Seattle, July 2008.
122. V. Nagarajan, D. Jeffrey, R. Gupta, and N. Gupta, "ONTRAC: A System for Efficient ONLINE TRACing for Debugging," *International Conference on Software Maintenance (ICSM)*, pages 445-454, Paris, October 2007.

123. V. Nagarajan, R. Gupta, X. Zhang, M. Madou, B. De Sutter, and K. De Bosschere, "Matching Control Flow of Program Versions," *International Conference on Software Maintenance (ICSM)*, pages 84-93, Paris, October 2007.
124. S. Tallam, C. Tian, X. Zhang, and R. Gupta, "Enabling Tracing of Long-Running Multi-threaded Programs via Dynamic Execution Reduction," *International Symposium on Software Testing and Analysis (ISSTA)*, pages 207-218, London, July 2007.
125. X. Zhang, S. Tallam, N. Gupta, and R. Gupta, "Towards Locating Execution Omission Errors," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 415-424, San Diego, June 2007.
126. V. Nagarajan, R. Gupta, and A. Krishnaswamy, "Compiler-Assisted Memory Encryption for Embedded Processors," *International Conference on High Performance Embedded Architectures and Compilers (HiPEAC)*, Springer Verlag, LNCS 4367, pages 7-22, Ghent, Belgium, January 2007.
127. X. Zhang, S. Tallam, and R. Gupta, "Dynamic Slicing Long Running Programs through Execution Fast Forwarding," *ACM SIGSOFT Symposium on Foundations of Software Engineering (FSE)*, pages 81-91, Portland, Oregon, November 2006.
128. H. Liu and R. Gupta, "Temporal Analysis of Routing Activity for Anomaly Detection in Ad hoc Networks," *IEEE International Conference on Mobile Ad-hoc and Sensor Systems (MASS)*, pages 505-508, October 2006.
129. X. Zhang, N. Gupta, and R. Gupta, "Pruning Dynamic Slices With Confidence," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 169-180, Ottawa, Canada, June 2006.
130. X. Zhang, N. Gupta, and R. Gupta, "Locating Faults Through Automated Predicate Switching," *IEEE/ACM International Conference on Software Engineering (ICSE)*, pages 272-281, Shanghai, China, May 2006.
131. A. Krishnaswamy and R. Gupta, "Efficient Use of Invisible Registers in Thumb Code," *IEEE/ACM 37th International Symposium on Microarchitecture (MICRO)*, pages 30-40, Barcelona, Spain, November 2005.
132. N. Gupta, H. He, X. Zhang, and R. Gupta, "Locating Faulty Code Using Failure-Inducing Chops," *IEEE/ACM International Conference on Automated Software Engineering (ASE)*, pages 263-272, Long Beach, California, November 2005.
133. X. Zhang and R. Gupta, "Matching Execution Histories of Program Versions," *Joint 10th European Software Engineering Conference and ACM SIGSOFT 13th Symposium on Foundations of Software Engineering (ESEC-FSE)*, pages 197-206, Lisbon, Portugal, September 2005.
134. X. Zhang, H. He, N. Gupta, and R. Gupta, "Experimental Evaluation of Using Dynamic Slices for Fault Location," *SIGSOFT-SIGPLAN Sixth International Symposium on Automated and Analysis-Driven Debugging (AADEBUB)*, pages 33-42, Monterey, California, September 2005.
135. S. Tallam, R. Gupta, and X. Zhang, "Extended Whole Program Paths," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pages 17-26, St. Louis, Missouri, September 2005.
136. B. Li, G. Venkatesh, B. Calder, and R. Gupta, "Exploiting a Computation Reuse Cache to Reduce Energy in Network Processor," *International Conference on High Performance Embedded Architectures and Compilers (HiPEAC)*, LNCS 3793, Springer Verlag, pages 251-265, Barcelona, Spain, September 2005.

137. Y. Zhang, L. Gao, J. Yang, X. Zhang, and R. Gupta, "SENS: Security Enhancement to Symmetric Shared Memory Multiprocessors," *IEEE 11th International Symposium on High Performance Computer Architecture (HPCA)*, pages 352-362, San Francisco, California, February 2005.
138. X. Zhang and R. Gupta, "Whole Execution Traces," *IEEE/ACM 37th International Symposium on Microarchitecture (MICRO)*, pages 105-116, Portland, Oregon, December 2004.
139. H. Liu and R. Gupta, "Selective Backbone Construction for Topology Control," *IEEE International Conference on Mobile Ad-hoc and Sensor Systems (MASS)*, pages 41-50, Fort Lauderdale, Florida, October 2004.
140. X. Zhang and R. Gupta, "Cost Effective Dynamic Program Slicing," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 94-106, Washington D.C., June 2004.
141. X. Zhang, R. Gupta, and Y. Zhang, "Efficient Forward Computation of Dynamic Slices Using Reduced Ordered Binary Decision Diagrams," *IEEE/ACM International Conference on Software Engineering (ICSE)*, pages 502-511, Edinburgh, UK, May 2004.
142. R. Bodik, R. Gupta, and M.L. Soffa, "Retrospective - Complete Removal of Redundant Expressions," *20 Years of the ACM/SIGPLAN Conference on Programming Language Design and Implementation (1979-1999): A Selection*, ACM SIGPLAN Notices, Vol. 39, No. 4, pages 596-597, April 2004.
143. S. Tallam, X. Zhang, and R. Gupta, "Extending Path Profiling across Loop Backedges and Procedure Boundaries," *Second Annual IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pages 251-262, San Jose, CA, March 2004.
144. B. Li and R. Gupta, "Simple Offset Assignment in Presence of Subword Data," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pages 12-23, San Jose, CA, October 2003.
145. Y. Zhang and R. Gupta, "Enabling Partial Cache Line Prefetching Through Data Compression," *International Conference on Parallel Processing (ICPP)*, pages 277-285, Kaohsiung, Taiwan, October 2003 **Recipient of the Most Original Paper Award.**
146. A. Krishnaswamy and R. Gupta, "Enhancing the Performance of 16-bit Code Using Augmenting Instructions," *ACM SIGPLAN Conference on Languages Compilers and Tools for Embedded Systems (LCTES)*, pages 254-264, San Diego, CA, June 2003. *One of four LCTES'03 papers invited for a special issue of ACM TECS.*
147. W-K. Chen, B. Li, and R. Gupta, "Code Compaction of Matching Single-Entry Multiple-Exit Regions," *10th Annual International Static Analysis Symposium (SAS)*, LNCS 2694, Springer Verlag, pages 401-417, San Diego, CA, June 2003.
148. X. Zhang, R. Gupta, and Y. Zhang, "Precise Dynamic Slicing Algorithms," *IEEE/ACM International Conference on Software Engineering (ICSE)*, pages 319-329, Portland, Oregon, May 2003. **Recipient of a Distinguished Paper Award.**
149. X. Zhang and R. Gupta, "Hiding Program Slices for Software Security," *1st Annual IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pages 325-336, San Francisco, CA, March 2003.
150. S. Tallam and R. Gupta, "Bitwidth Aware Global Register Allocation." *30th Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL)*, pages 85-96, New Orleans, LA, January 2003.

151. J. Yang and R. Gupta, "Energy Efficient Frequent Value Data Cache Design," *IEEE/ACM 35th International Symposium on Microarchitecture (MICRO)*, pages 197-207, Istanbul, Turkey, November 2002.
152. B. Li and R. Gupta, "Bit Section Instruction Set Extension of ARM for Embedded Applications," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pages 69-78, Grenoble, France, October 2002.
153. A. Krishnaswamy and R. Gupta, "Profile Guided Selection of ARM and Thumb Instructions," *ACM SIGPLAN Joint Conference on Languages Compilers and Tools for Embedded Systems & Software and Compilers for Embedded Systems (LCTES)*, pages 55-63, Berlin, Germany, June 2002.
154. R. Gupta, E. Mehofer, and Y. Zhang, "A Representation for Bit Section based Analysis and Optimization," *International Conference on Compiler Construction (CC)*, LNCS 2304, Springer Verlag, pages 62-77, Grenoble, France, April 2002.
155. Y. Zhang and R. Gupta, "Data Compression Transformations for Dynamically Allocated Data Structures," *International Conference on Compiler Construction (CC)*, LNCS 2304, Springer Verlag, pages 14-28, Grenoble, France, April 2002.
156. S. Rele, S. Pande, S. Onder and R. Gupta, "Optimization of Static Power Dissipation by Functional Units in Superscalar Processors," *International Conference on Compiler Construction (CC)*, LNCS 2304, Springer Verlag, pages 261-275, Grenoble, France, April 2002.
157. Y. Zhang and R. Gupta, "Path Matching in Compressed Control Flow Traces," *Data Compression Conference (DCC)*, pages 132-141, Snowbird, Utah, April 2002.
158. S. Onder and R. Gupta, "Instruction Wake-Up in Wide Issue Superscalars," *7th European Conference on Parallel Computing (EuroPar)*, LNCS 2150, Springer Verlag, pages 418-427, Manchester, UK, August 2001.
159. J. Yang and R. Gupta, "FV Encoding for Low-Power Data I/O," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pages 84-87, Huntington Beach, CA, August 2001.
160. J. Yang and R. Gupta, "Energy-Efficient Load and Store Reuse," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pages 72-75, Huntington Beach, CA, August 2001.
161. Y. Zhang and R. Gupta, "Timestamped Whole Program Path Representation and its Applications," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 180-190, Snowbird, Utah, June 2001.
162. S. Onder and R. Gupta, "Load and Store Redundancy Removal Using Register File Contents," *ACM 15th International Conference on Supercomputing (ICS)*, pages 289-302, Sorrento, Naples, Italy, June 2001.
163. J. Yang, Y. Zhang, and R. Gupta, "Frequent Value Compression in Data Caches," *IEEE/ACM 33rd International Symposium on Microarchitecture (MICRO)*, pages 258-265, Monterey, CA, December 2000.
164. Y. Zhang, J. Yang, and R. Gupta, "Frequent Value Locality and Value-Centric Data Cache Design," *ACM 9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 150-159, Cambridge, MA, November 2000.
165. J. Yang and R. Gupta, "Load Redundancy Removal through Instruction Reuse," *International Conference on Parallel Processing (ICPP)*, pages 61-68, Toronto, Canada, August 2000.

166. R. Bodik, R. Gupta, and V. Sarkar, "ABCD: Eliminating Array Bounds Checks on Demand," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 321-333, Vancouver B.C., Canada, June 2000.
167. C. Jaramillo, R. Gupta, and M.L. Soffa, "FULLDOC: A Full Reporting Debugger for Optimized Code," *International Static Analysis Symposium (SAS), LNCS 1824, Springer Verlag*, pages 240-259, Santa Barbara, CA, June-July 2000.
168. S. Onder and R. Gupta, "Dynamic Memory Disambiguation in the Presence of Out-of-order Store Issuing," *IEEE/ACM 32nd International Symposium on Microarchitecture (MICRO)*, pages 170-176, Haifa, Israel, November 1999.
169. S. Onder, J. Xu, and R. Gupta, "Caching and Predicting Branch Sequences for Improved Fetch Effectiveness," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pages 294-302, Newport Beach, California, October 1999.
170. C. Jaramillo, R. Gupta, and M.L. Soffa, "Comparison Checking: An Approach to Avoid Debugging of Optimized Code," *Joint 7th European Software Engineering Conference and ACM SIGSOFT 7th Symposium on Foundations of Software Engineering (ESEC-FSE), LNCS 1687, Springer Verlag*, pages 268-284, Toulouse, France, Sept. 1999.
171. R. Bodik, R. Gupta, and M.L. Soffa, "Load-Reuse Analysis: Design and Evaluation," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 64-76, Atlanta, Georgia, May 1999.
172. T. Nakra, R. Gupta, and M.L. Soffa, "Value Prediction in VLIW Machines," *ACM/IEEE 26th International Symposium on Computer Architecture (ISCA)*, pages 258-269, Atlanta, Georgia, May 1999.
173. X. Yuan, R. Gupta and R. Melhem, "Compiler Analysis to Support Compiled Communication for HPF-like Programs," *13th International Parallel Processing Symposium and 10th Symposium on Parallel and Distributed Processing (IPPS/SPDP)*, pages 603-608, San Juan, Puerto Rico, April 1999.
174. R. Gupta and R. Bodik, "Register Pressure Sensitive Redundancy Elimination," *International Conference on Compiler Construction (CC), LNCS 1575, Springer Verlag*, pages 107-121, Amsterdam, Netherlands, March 1999.
175. T. Nakra, R. Gupta, and M.L. Soffa, "Global Context-based Value Prediction," *IEEE International Symposium on High Performance Computer Architecture (HPCA)*, pages 4-12, Orlando, Florida, January 1999.
176. C. Jaramillo, R. Gupta, and M.L. Soffa, "Capturing the Effects of Code Improving Transformations," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pages 118-123, Paris, France, October 1998.
177. S. Onder and R. Gupta, "Superscalar Execution with Direct Data Forwarding," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pages 130-135, Paris, France, October 1998.
178. X. Yuan, R. Melhem and R. Gupta, "Performance of Multihop Communications Using Logical Topologies on Optical Torus Networks," *7th International Conference on Computer Communications and Networks (IC3N)*, pages 494-501, Lafayette, Louisiana, October 1998.
179. W. Wu, R. Gupta, and M. Spezialetti, "Experimental Evaluation of On-line Techniques for Removing Monitoring Intrusion," *SIGMETRICS 2nd Symposium on Parallel and Distributed Tools (SPDT)*, pages 30-39, Oregon, August 1998.

180. R. Bodik, R. Gupta, and M.L. Soffa, "Complete Removal of Redundant Expressions," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 1-14, Montreal, Canada, June 1998. *Included in 20 Years of PLDI (1979-1999): A Selection.*
181. S. Onder and R. Gupta, "Automatic Generation of Microarchitecture Simulators," *IEEE International Conference on Computer Languages (ICCL)*, pages 80-89, Chicago, Illinois, May 1998.
182. R. Gupta, D. Berson, and J.Z. Fang, "Path Profile Guided Partial Redundancy Elimination Using Speculation," *IEEE International Conference on Computer Languages (ICCL)*, pages 230-239, Chicago, Illinois, May 1998.
183. W. Wu, M. Spezialetti, and R. Gupta, "A Protocol for Removing Communication Intrusion in Monitored Distributed Systems," *IEEE-CS 18th International Conference on Distributed Computing Systems (ICDCS)*, pages 120-129, Tilburg, The Netherlands, May 1998.
184. R. Gupta, "A Code Motion Framework for Global Instruction Scheduling," *International Conference on Compiler Construction (CC)*, LNCS 1383, Springer Verlag, pages 219-233, Lisbon, Portugal, March 1998.
185. R. Gupta, D. Berson, and J.Z. Fang, "Resource-Sensitive Profile-Directed Data Flow Analysis for Code Optimization," *IEEE/ACM 30th International Symposium on Microarchitecture (MICRO)*, pages 358-368, Research Triangle Park, North Carolina, December 1997.
186. R. Gupta, "Code Optimization as a Side Effect of Instruction Scheduling," *International Conference on High Performance Computing (HiPC)*, pages 370-377, Bangalore, India, December 1997 (invited paper).
187. R. Gupta, D. Berson, and J.Z. Fang, "Path Profile Guided Partial Dead Code Elimination Using Predication," *International Conference on Parallel Architectures and Compilation Techniques (FACT)*, pages 102-115, San Francisco, California, November 1997.
188. W. Wu, M. Spezialetti, and R. Gupta, "On-line Avoidance of Communication Intrusion in Token Ring Networks," *IASTED 9th International Conference on Parallel and Distributed Computing and Systems (PDCS)*, pages 429-436, Washington, D.C., October 1997.
189. R. Bodik, R. Gupta, and M.L. Soffa, "Refining Data Flow Information using Infeasible Paths," *Joint 6th European Software Engineering Conference and ACM SIGSOFT 5th Symposium on Foundations of Software Engineering (ESEC-FSE)*, LNCS 1301, Springer Verlag, pages 361-377, Zurich, Switzerland, Sept. 1997.
190. R. Bodik and R. Gupta, "Partial Dead Code Elimination using Slicing Transformations," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 159-170, Las Vegas, Nevada, June 1997.
191. R. Bodik, R. Gupta, and M.L. Soffa, "Interprocedural Conditional Branch Elimination," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 146-158, Las Vegas, Nevada, June 1997.
192. X. Yuan, R. Melhem, and R. Gupta, "Distributed Path Reservation Algorithms for Multiplexed All-Optical Interconnection Networks," *IEEE 3rd International Symposium on High-Performance Computer Architecture (HPCA)*, pages 38-47, San Antonio, Texas, February 1997.
193. X. Yuan, R. Melhem, and R. Gupta, "Compiled Communication for All-Optical TDM Networks," *Supercomputing (SC)*, Article No. 25, 15 pages, Pittsburgh, Pennsylvania, November 1996.

194. W. Wu, M. Spezialetti, and R. Gupta, "Guaranteed Intrusion Removal from Monitored Distributed Applications," *IEEE 8th Symposium on Parallel and Distributed Processing (SPDP)*, pages 422-425, New Orleans, Louisiana, October 1996.
195. W. Wu, M. Spezialetti, and R. Gupta, "Designing a Non-intrusive Monitoring Tool for Developing Complex Distributed Applications," *IEEE 2nd International Conference on Engineering of Complex Computer Systems (ICECCS)*, pages 450-457, Montreal, Canada, October 1996. **Recipient of the Outstanding Paper Award.**
196. X. Yuan, R. Gupta, and R. Melhem, "Distributed Control in Optical WDM Networks," *IEEE Conference on Military Communication (MILCOM)*, pages 100-104, McLean, VA, October 1996.
197. X. Yuan, R. Melhem, and R. Gupta, "A Timestamp-based Selective Invalidation Scheme for Multiprocessor Cache Coherence," *International Conference on Parallel Processing (ICPP)*, Vol. III, pages 114-121, Bloomingdale, Illinois, August 1996.
198. W. Wu, M. Spezialetti, and R. Gupta, "On-line Avoidance of the Intrusive Affects of Monitoring on Runtime Scheduling Decisions," *IEEE-CS 16th International Conference on Distributed Computing Systems (ICDCS)*, pages 216-223, Hong Kong, May 1996.
199. R. Gupta, D. Mossé, and R. Suchoza, "Real-Time Scheduling using Compact Task Graphs," *IEEE-CS 16th International Conference on Distributed Computing Systems (ICDCS)*, pages 55-63, Hong Kong, May 1996.
200. E. Duesterwald, R. Gupta, and M.L. Soffa, "A Demand-Driven Analyzer for Data Flow Testing at the Integration Level," *IEEE/ACM International Conference on Software Engineering (ICSE)*, pages 575-586, Berlin, Germany, March 1996.
201. S. Onder and R. Gupta, "SINAN - A Forwarding Multithreaded Architecture," *International Conference on High Performance Computing (HiPC)*, pages 347-354, New Delhi, India, December 1995.
202. R. Gupta and M.L. Soffa, "Hybrid Slicing: An Approach for Refining Static Slices using Dynamic Information," *ACM SIGSOFT 3rd Symposium on the Foundations of Software Engineering (FSE)*, pages 29-40, Washington, DC, October 1995.
203. R. Gupta and M.L. Soffa, "Priority Based Data Flow Testing," *IEEE-CS International Conference on Software Maintenance (ICSM)*, pages 348-357, Nice, France, October 1995.
204. R. Gupta and R. Bodik, "Adaptive Loop Transformations for Scientific Programs," *IEEE Symposium on Parallel and Distributed Processing (SPDP)*, pages 368-375, San Antonio, Texas, October 1995.
205. R. Gupta and M. Spezialetti, "Dynamic Techniques for Minimizing the Intrusive Affects of Monitoring Actions," *IEEE-CS 15th International Conference on Distributed Computing Systems (ICDCS)*, pages 368-376, Vancouver, Canada, June 1995.
206. E. Duesterwald, R. Gupta, and M.L. Soffa, "Demand-driven Computation of Interprocedural Data Flow," *22nd Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL)*, pages 37-48, San Francisco, California, January 1995.
207. R. Gupta and M. Spezialetti, "Busy-Idle Profiles and Compact Task Graphs: Compile-time Support for Interleaved and Overlapped Scheduling of Real-Time Tasks," *IEEE 15th Real-Time Systems Symposium (RTSS)*, pages 86-96, San Juan, Puerto Rico, December 1994.
208. M. Spezialetti and R. Gupta, "Exploiting Program Semantics for Efficient Instrumentation of Distributed Event Recognitions," *IEEE 13th Symposium on Reliable Distributed Systems (SRDS)*, pages 181-191, Dana Point, California, October 1994.

209. R. Gupta and M.L. Soffa, "A Framework for Partial Data Flow Analysis," *IEEE-CS International Conference on Software Maintenance (ICSM)*, pages 4-13, Victoria, British Columbia, September 1994.
210. D. Berson, R. Gupta, and M.L. Soffa, "Resource Spackling: A Framework for Integrating Register Allocation in Local and Global Schedulers," *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, *IFIP Transactions A-50*, pages 135-146, Montreal, Canada, August 1994.
211. M. Spezialetti and R. Gupta, "Perturbation Analysis: A Static Analysis Approach for the Non-Intrusive Monitoring of Parallel Programs," *International Conference on Parallel Processing (ICPP)*, Vol. II, pages 81-88, St. Charles, Illinois, August 1994.
212. M. Spezialetti and R. Gupta, "Debugging Distributed Programs through the Detection of Simultaneous Events," *IEEE-CS 14th International Conference on Distributed Computing Systems (ICDCS)*, pages 634-641, Poznan, Poland, June 1994.
213. C. Gong, R. Melhem, and R. Gupta, "Compiler Assisted Fault Detection for Distributed-Memory Systems," *IEEE Scalable High Performance Computing Conference (SHPCC)*, pages 373-380, Knoxville, Tennessee, May 1994.
214. E. Duesterwald, R. Gupta, and M.L. Soffa, "Reducing the Cost of Data Flow Analysis By Congruence Partitioning," *International Conference on Compiler Construction (CC)*, *LNCS 786 Springer Verlag*, pages 357-373, Edinburgh, Great Britain, April 1994.
215. C. Gong, R. Gupta, and R. Melhem, "Compilation Techniques for Communication Optimizations on Distributed Memory Systems," *International Conference on Parallel Processing (ICPP)*, Vol. II, pages 39-46, St. Charles, Illinois, August 1993.
216. E. Duesterwald, R. Gupta, and M.L. Soffa, "A Practical Data Flow Framework for Array Reference Analysis and its Application in Optimizations," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 68-77, Albuquerque, New Mexico, June 1993.
217. D. Berson, R. Gupta, and M.L. Soffa, "URSA: A Unified ReSource Allocator for Registers and Functional Units in VLIW Architectures," *Conference on Architectures and Compilation Techniques for Fine and Medium Grain Parallelism (PACT)*, *IFIP Transactions A-23*, pages 243-254, Orlando, Florida, January 1993.
218. B. Malloy, R. Gupta, and M.L. Soffa, "A Shape Matching Approach for Scheduling Fine-Grained Parallelism," *IEEE/ACM 25th International Symposium on Microarchitecture (MICRO)*, pages 264-267, Portland, Oregon, December 1992.
219. R. Gupta, M.J. Harrold, and M.L. Soffa, "An Approach to Regression Testing using Slicing," *IEEE-CS International Conference on Software Maintenance (ICSM)*, pages 299-308, Orlando, Florida, November 1992.
220. T. Watts, M.L. Soffa, and R. Gupta, "Techniques for Integrating Parallelizing Transformations and Compiler Based Scheduling Methods," *Supercomputing (SC)*, pages 830-839, Minneapolis, Minnesota, November 1992.
221. R. Gupta and M.L. Soffa, "Automatic Generation of a Compact Test Suite," *12th IFIP World Computer Congress (IFIP)*, Vol. I, pages 237-243, Madrid, Spain, September 1992.
222. R. Gupta, "SPMD Execution of Programs with Dynamic Data Structures on Distributed Memory Machines," *IEEE 4th International Conference on Computer Languages (ICCL)*, pages 232-241, Oakland, California, April 1992.
223. R. Gupta, "Compiler Optimizations for Distributed-Memory Programs," *Scalable High Performance Computing Conference (SHPCC)*, pages 178-181, Williamsburg, Virginia, April 1992.

224. E. Duesterwald, R. Gupta, and M.L. Soffa, "Rigorous Data Flow Testing through Output Influences," *2nd Irvine Software Symposium (ISS)*, pages 131-145, Univ. of California, Irvine, CA, March 1992.
225. R. Kramer, R. Gupta, and M.L. Soffa, "The Combining DAG: A Technique for Parallel Data Flow Analysis," *6th International Parallel Processing Symposium (IPPS)*, pages 652-655, Beverly Hills, California, March 1992.
226. R. Gupta, "Generalized Dominators and Post-Dominators," *18th Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL)*, pages 246-257, Albuquerque, New Mexico, January 1992.
227. S. Lee and R. Gupta, "Executing Loops on a Fine-Grained MIMD Architecture," *IEEE/ACM 24th International Symposium on Microarchitecture (MICRO)*, pages 199-205, Albuquerque, New Mexico, November 1991.
228. R. Gupta and M. Spezialetti, "Loop Monotonic Computations: An Approach for the Efficient Run-time Detection of Races," *SIGSOFT Symposium on Testing, Analysis, and Verification (TAVS)*, pages 98-111, Victoria, Canada, October 1991.
229. P. Gopinath and R. Gupta, "A Hybrid Approach to Load Balancing in Distributed Systems," *Symposium on Experiences with Distributed and Multiprocessor Systems (SEDMS)*, pages 133-147, Atlanta, March 1991.
230. P. Gopinath and R. Gupta, "Applying Compiler Techniques to Scheduling in Real Time Systems," *IEEE 11th Real-Time Systems Symposium (RTSS)*, pages 247-256, Orlando, Florida, December 1990.
231. R. Gupta, M. Epstein, and M. Whelan, "The Design of a RISC based Multiprocessor Chip," *Supercomputing (SC)*, pages 920-929, New York, November 1990.
232. R. Gupta and Chi-Hung Chi, "Improving Instruction Cache Performance by Reducing Cache Pollution," *Supercomputing (SC)*, pages 82-91, New York, November 1990.
233. R. Gupta, "Loop Displacement: An Approach for Transforming and Scheduling Loops for Parallel Execution," *Supercomputing (SC)*, pages 388-397, New York, November 1990.
234. M.J. Harrold, R. Gupta, and M.L. Soffa, "A Methodology for Controlling the Size of a Test Suite," *IEEE-CS International Conference on Software Maintenance (ICSM)*, pages 302-310, San Diego, CA, November 1990.
235. R. Gupta, "A Fresh Look at Optimizing Array Bound Checking," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 272-282, White Plains, New York, June 1990.
236. M.J. Harrold, R. Gupta, and M.L. Soffa, "TBM: A Testbed Management Tool," *7th International Conference on Testing Computer Software*, pages 47-56, San Francisco, California, June 1990.
237. P. Gopinath and R. Gupta, "Opportunistic Evaluation of Communication Link Loads," *IEEE-CS 10th International Conference on Distributed Computing Systems (ICDCS)*, pages 406-413, Paris, France, May 1990.
238. R. Gupta and P. Gopinath, "A Hierarchical Approach to Load Balancing in Distributed Systems," *5th Distributed Memory Computing Conference (DMCC)*, pages 1000-1005, Vol. II, Charleston, South Carolina, April 1990.
239. R. Gupta, "Employing Register Channels for the Exploitation of Instruction Level Parallelism," *ACM SIGPLAN 2nd Symposium on Principles and Practice of Parallel Programming (PPoPP)*, pages 118-127, Seattle, Washington, March 1990.

240. R. Gupta, "Synchronization and Communication Costs of Loop Partitioning on Shared-Memory Multiprocessor Systems," *International Conference on Parallel Processing (ICPP)*, Vol. II, pages 23-30, St. Charles, Illinois, August 1989.
241. R. Gupta, M.L. Soffa, and T.F. Steele, "Register Allocation via Clique Separators," *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 264-275, Portland, Oregon, June 1989.
242. R. Gupta and M. Epstein, "Achieving Low Cost Synchronization in a Multiprocessor System," *Conference on Parallel Architectures and Languages Europe (PARLE)*, Vol. I, pages 70-84, Eindhoven, The Netherlands, June 1989.
243. R. Gupta, "The Fuzzy Barrier: A Mechanism for High-Speed Synchronization of Processors," *ACM 3rd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 54-64, Boston, April 1989.
244. T.S. Anand and R. Gupta, "A Knowledge-based Tool for Parallelization of Scientific Programs," *IMACS Conference on Expert Systems in Numerical Computation*, Purdue University, Indiana, December 1988.
245. R. Gupta and M.L. Soffa, "Compile-time Techniques for Efficient Utilization of Parallel Memories," *ACM SIGPLAN Symposium on Parallel Programming: Experience with Applications, Languages and Systems (PPEALS)*, pages 235-246, New Haven, July 1988.
246. R. Gupta, "Debugging Code Reorganized by a Trace Scheduling Compiler," *3rd International Conference on Supercomputing*, Boston, Vol. III, pages 422-430, May 1988.
247. R. Gupta and M.L. Soffa, "A Matching Approach to Utilizing Fine-Grained Parallelism," *21st Annual Hawaii International Conference on System Sciences (HICSS)*, Vol. I, pages 148-156, Kona, Hawaii, January 1988.
248. R. Gupta and M.L. Soffa, "A Reconfigurable LIW Architecture," *International Conference on Parallel Processing (ICPP)*, pages 893-900, St. Charles, Illinois, August 1987.
249. R. Gupta and M.L. Soffa, "Region Scheduling," *2nd International Conference on Supercomputing*, Vol. III, pages 141-148, Santa Clara, May 1987.
250. R. Gupta and M.L. Soffa, "SHAPE: A Highly Adaptable and Parallel System," *Computer Science Conference*, pages 107-114, Cincinnati, February 1986.
251. R. Gupta and M.L. Soffa, "The Efficiency of Storage Management Schemes for Ada Programs," *Ada International Conference*, pages 164-172, Paris, May 1985. Also published in *Sigplan Notices*, Vol. 20, No. 11, pages 30-38, November 1985.

WORKSHOP PUBLICATIONS

252. H. Li, Z. Chen, R. Gupta, and M. Xie, "Non-Intrusively Avoiding Scaling Problems in and out of MPI Collectives," *International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS)*, pages 415-424, in IEEE IPDPSW Proceedings, Vancouver, British Columbia, Canada, May 2018.
253. F. Khorasani, K. Vora, R. Gupta, and L.N. Bhuyan, "Enabling Work-Efficiency for High Performance Vertex-Centric Graph Analytics on GPUs," *Seventh Workshop on Irregular Applications: Architectures and Algorithms (IA³)*, Article No. 11, 4 pages, Denver, Colorado, November 2017.
254. S.C. Koduru, R. Gupta, and I. Neamtiu, "Size Oblivious Programming with *InfiniMem*," *The 28th International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 9519, Springer, Chapter 1, pages 3-19, Raleigh, North Carolina, Sept. 2015. **Recipient of the Best Student Paper Award.**

255. A. Kusum, I. Neamtiu, and R. Gupta, "Adapting Graph Application Performance Via Alternate Data Structure Representations," *5th International Workshop on Adaptive Self-tuning Computing Systems (ADAPT)*, 7 pages, Amsterdam, The Netherlands, January 2015.
256. M. Feng, F. Khorasani, R. Gupta, and L.N. Bhuyan, "LightPlay: Efficient Replay with GPUs," *The 27th International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 8967, Springer, Chapter 22, pages 332-347, Hillsboro, Oregon, Sept. 2014.
257. M. Feng, R. Gupta, and L.N. Bhuyan, "Optimistic Parallelism on GPUs," *The 27th International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 8967, Springer, Chapter 1, pages 3-18, Hillsboro, Oregon, September 2014.
258. M. Belviranli, C. Chou, L.N. Bhuyan, and R. Gupta, "A Paradigm Shift in GP-GPU Computing: Task Based Execution of Applications with Dynamic Data Dependences," *The 6th International Workshop on Data-intensive Distributed Computing (DIDC)*, pages 29-34, June 2014.
259. S-C. Koduru, K. Vora, and R. Gupta, " ABC^2 : Adaptively Balancing Computation & Communication in a DSM cluster of Multicores for Irregular Applications," *International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS)*, pages 391-400, in IEEE IPDPSW Proceedings, Phoenix, Arizona, May 2014.
260. M. Feng, R. Gupta, and I. Neamtiu, "Programming Support for Speculative Execution with Software Transactional Memory," *International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS)*, pages 394-403, in IEEE IPDPSW Proceedings, Boston, Massachusetts, May 2013.
261. M. Feng, C. Tian, and R. Gupta, "Enhancing LRU Replacement via Phantom Associativity," *Workshop on Interaction between Compilers and Computer Architectures (INTERACT)*, 8 pages, Feb. 2012.
262. M. Feng and R. Gupta, "Learning Universal Probabilistic Models for Fault Localization," *Ninth ACM SIGPLAN-SIGSOFT Workshop on Program Analysis for Software Tools and Engineering (PASTE)*, pages 81-88, June 2010.
263. V. Nagarajan and R. Gupta, "Speculative Optimizations for Parallel Programs on Multicores," *22nd International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 5898/2010, pages 323-337, Newark, Delaware, October 2009.
264. V. Nagarajan and R. Gupta, "Support for Symmetric Shadow Memory in Multiprocessors," *Workshop on Parallel and Distributed Systems: Testing, Analysis, and Debugging (PADTAD)*, 9 pages, July 2008.
265. C. Tian, V. Nagarajan, and R. Gupta, "Synchronization Aware Conflict Resolution for Runtime Monitoring Using Transactional Memory," *Workshop on Software Tools for Multicore Systems (STMCS)*, 6 pages, April 2008.
266. R. Gupta, N. Gupta, X. Zhang, D. Jeffrey, V. Nagarajan, S. Tallam and C. Tian, "Scalable Dynamic Information Flow Tracking and its Applications," *NSF Next Generation Software Workshop (NSFNCS)*, 5 pages, April 2008.
267. V. Nagarajan, H-S. Kim, Y. Wu, and R. Gupta, "Dynamic Information Flow Tracking on Multicores," *Workshop on Interaction between Compilers and Computer Architectures (INTERACT)*, 10 pages, Feb. 2008.
268. N. Gupta and R. Gupta, "ExPert: Dynamic Analysis based Fault Location via Execution Perturbations," *NSF Next Generation Software Workshop (NSFNCS)*, 6 pages, March 2007.

269. B. Li, Y. Zhang, and R. Gupta, "Speculative Subword Register Allocation in Embedded Processors," *The 17th International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 3602, Springer Verlag, pages 56-71, West Lafayette, Indiana, September 2004.
270. S. Tallam and R. Gupta, "Profile-Guided Java Program Partitioning for Power Aware Computing," *Sixth International Workshop on Java for Parallel and Distributed Computing*, Sante Fe, NM, April 2004.
271. C. Jaramillo, R. Gupta, and M.L. Soffa, "Verifying Optimizers through Comparison Checking," *International Workshop on Compiler Optimization Meets Compiler Verification (COCV)*, in conjunction with ETAPS, Grenoble, France, April 2002.
272. D. Berson, R. Gupta, and M.L. Soffa, "An Evaluation of Integrated Scheduling and Register Allocation Techniques," *11th International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 1239, Springer Verlag, pages 207-221, North Carolina, Chapel Hill, August 1998.
273. J. Tims, R. Gupta, and M.L. Soffa, "Dataflow Analysis Driven Dynamic Data Partitioning," *4th Workshop on Languages, Compilers, and Run-time Systems for Scalable Computers*, LNCS 1511, Springer Verlag, pages 75-90, Pittsburgh, PA, May 1998.
274. X. Yuan, R. Gupta, and R. Melhem, "An Array Data Flow Analysis based Communication Optimizer," *10th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 1366, Springer Verlag, pages 246-260, Minneapolis, Minnesota, August 1997.
275. X. Yuan, R. Gupta, and R. Melhem, "Does Time Division Multiplexing Close the Gap between Memory and Optical Communication Speeds," *Workshop on Parallel Computing, Routing, and Communication*, LNCS 1417, Springer Verlag, pages 261-271, Atlanta, Georgia, June 1997.
276. X. Yuan, R. Gupta, and R. Melhem, "Demand-Driven Data Flow Analysis for Communication Optimization," *Workshop on Challenges in Compiling for Scalable Parallel Systems*, New Orleans, Louisiana, October 1996 (invited paper).
277. D. Berson, P. Chang, R. Gupta and M.L. Soffa, "Integrating Program Optimizations and Transformations with the Scheduling of Instruction Level Parallelism," *9th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 1239, Springer Verlag, pages 207-221, Santa Clara, California, August 1996.
278. R. Bodik and R. Gupta, "Array Data-Flow Analysis for Load-Store Optimizations in Superscalar Architectures," *8th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 1033 Springer Verlag, pages 1-15, Columbus, Ohio, August 1995.
279. D. Berson, R. Gupta, and M.L. Soffa, "GURRR: A Global Unified Resource Requirements Representation," *ACM SIGPLAN Workshop on Intermediate Representations*, pages 23-34, San Francisco, California, January 1995.
280. C. Gong, R. Melhem, and R. Gupta, "Replicating Statement Execution for Fault Detection on Distributed Memory Multiprocessors," *IEEE Fault-Tolerant Parallel and Distributed Systems Workshop*, pages 132-141, College Station, Texas, June 1994.
281. M. Spezialetti and R. Gupta, "Timed Perturbation Analysis: An Approach for Non-Intrusive Monitoring of Real Time Computations," *ACM SIGPLAN Workshop on Language, Compiler, and Tool Support for Real-Time Systems (LCT-RTS)*, pages 1-11, Orlando, Florida, June 1994.
282. R. Gupta and P. Gopinath, "Correlation Analysis Techniques for Refining Execution Time Estimates of Real-Time Applications," *IEEE 11th Workshop on Real-Time Operating Systems and Software (RTOS)*, pages 54-58, Seattle, Washington, May 1994.

283. R. Gupta and M. Spezialetti, "Towards a Non-Intrusive Approach for Monitoring Distributed Computations through Perturbation Analysis," *6th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 768 Springer Verlag, pages 586-601, Portland, Oregon, August 1993.
284. P. Gopinath, T. Bihari, and R. Gupta, "Supporting Real-Time Software Integrated Circuits," *IEEE Workshop on Imprecise and Approximate Computation*, pages 55-61, Phoenix, Arizona, December 1992.
285. E. Duesterwald, R. Gupta, and M.L. Soffa, "Register Pipelining: An Integrated Approach to Register Allocation for Scalar and Subscripted Variables," *International Workshop on Compiler Construction (CC)*, LNCS 641 Springer Verlag, pages 192-206, Paderborn, Germany, October 1992.
286. E. Duesterwald, R. Gupta, and M.L. Soffa, "Distributed Slicing and Partial Re-execution for Distributed Programs," *5th Workshop on Languages and Compilers for Parallel Computing (LCPC)*, LNCS 757 Springer Verlag, pages 497-511, Yale University, New Haven, Connecticut, August 1992.
287. P. Gopinath, T. Bihari, and R. Gupta, "Compiler Techniques for Generating Predictable Object-Oriented Real-Time Software," *IEEE 9th Workshop on Real-Time Operating Systems and Software (RTOSS)*, Pittsburgh, May 1992.
288. R. Gupta, "A Fine-grained MIMD Architecture based upon Register Channels," *IEEE/ACM 23rd Workshop on Microprogramming and Microarchitecture (MICRO)*, pages 28-37, Orlando, Florida, Dec. 1990.
289. R. Gupta, L. Pollock, and M.L. Soffa, "Parallelizing Data Flow Analysis," *Workshop on Parallel Compilation*, Kingston, Ontario, May 1990.
290. P. Gopinath and R. Gupta, "Compiler Assisted Adaptive Scheduling in Real-time Systems," *IEEE Workshop on Real-Time Operating Systems and Software (RTOSS)*, *Real-Time Systems Newsletter*, Vol. 6, No. 2, pages 62-69, Univ. of Virginia, Charlottesville, VA, May 1990.

BOOK CONTRIBUTIONS

291. C. Tian, M. Feng, and R. Gupta, "Software Based Speculative Parallelization For Multi-core/Manycore Architecture," In *Programming Multi-core and Many-core Computing Systems*, John Wiley & Sons, Chapter 10, pages 205-225, Edited by S. Pllana & F. Khafa, Jan. 2017.
292. X. Zhang, N. Gupta, and R. Gupta, "Whole Execution Profiles and their Use in Debugging," *The Compiler Design Handbook: Optimizations and Machine Code Generation*, 2nd Edition, Chapter 4, CRC Press, pages 4-1-4-17, Editors: Y.N. Srikant & P. Shankar, Dec. 2007.
293. Y. Zhang and R. Gupta, "Enabling Partial Cache Line Prefetching Through Data Compression," *High Performance Computing: Paradigm and Infrastructure*, pages 183-200, John Wiley & Sons, Edited by L.T. Yang and M. Guo, October 2005.
294. N. Gupta and R. Gupta, "Data Flow Testing," *The Compiler Design Handbook: Optimizations and Machine Code Generation*, First Edition, Chapter 7, pages 247-267, CRC Press, Edited by Y.N. Srikant and P. Shankar, September 2002.
295. R. Gupta, E. Mehofer, and Y. Zhang, "Profile Guided Compiler Optimizations," *The Compiler Design Handbook: Optimizations and Machine Code Generation*, First Edition, Chapter 4, pages 143-174, CRC Press, Edited by Y.N. Srikant and P. Shankar, September 2002.
296. R. Gupta, "SPMD Execution in Presence of Dynamic Data Structures," *Compiler Optimizations for Scalable Parallel Systems: Languages, Compilation Techniques and Run Time Systems*, LNCS 1808, Springer, pages 683-706, Editors: S. Pande and D.P. Agrawal, 2001.

297. T.S. Anand and R. Gupta, "A Tool for Evaluating Compiler-based Parallelization Strategies," *Intelligent Mathematical Software Systems*, pages 103-110, Edited by E.N. Houstis, J.R. Rice, and R. Vichnevetsky, North Holland, 1990.

INVITED PRESENTATIONS

1. *Virginia Tech*, Blacksburg, **Distinguished Lecture Series Speaker**, "Parallel Graph Processing on Clusters, Multicores, and GPUs," to be presented November 2018.
2. *University of Southern California*, Los Angeles, "Parallel Graph Processing on GPUs, Clusters, and Multicores," September 2016.
3. *University of California*, Irvine, **EECS Distinguished Seminar Series Speaker**, "Parallel Graph Processing on GPUs and Clusters," March 2016.
4. *University of California*, Irvine, "Exploiting Parallelism on Multicores Via SpiceC," April 2013.
5. *4th Compiler Assisted SoC Assembly Workshop (CASA'08 - held at ESWEK)*, "Speculative Parallelization of Applications on Multicores," October 2008.
6. *Google*, Mountain View, "Speculative Parallelization of Applications on Multicores," October 2008.
7. *Workshop on Dynamic Analysis (WODA'07 - held at ICSE)*, **Keynote Speaker**, "Scalable Dynamic Analysis for Automated Fault Location and Avoidance," May 2007.
8. *University of California*, Davis, "Delivering Processor Performance with Limited Energy and Memory Resources," April 2007.
9. *Microsoft Research*, Redmond, "Scalable Dynamic Analysis for Automated Fault Location," March 2007.
10. *University of Colorado*, Boulder, "Reliable and Optimized Embedded Systems," March 2007.
11. *The College of William and Mary*, Williamsburg, VA, "Safety and Optimization of Embedded Systems," Jan. 2007.
12. *University of California*, Riverside, "Safety and Optimization of Embedded Systems," December 2006.
13. *Massachusetts Institute of Technology*, "Safety and Optimization of Embedded Systems," Joint EECS and Aeronautics & Astronautics Seminar, May 2006.
14. Taught a course on "Compiling for Embedded Processors," First HiPEAC Summer School on *Advanced Computer Architectures and Compilation for Embedded Systems (ACACES)*, L'Aquila, Italy, July 2005.
15. *Microsoft Research Faculty Summit*, "Using Phoenix for Exploring Whole Execution Traces," Redmond, Washington, July 2005.
16. *University of California*, San Diego, "Dynamic Execution Histories and their Applications," May 2005.
17. *Arizona State University*, Tempe, Arizona, "Whole Execution Trace and its Applications," December 2004.
18. *The College of William and Mary*, Williamsburg, VA, **Distinguished Lecture Series Speaker**, "Enabling the Design of Compilers and Architectures for Emerging Applications," October 2004.
19. *Microsoft Research Faculty Summit*, "Using Phoenix for Profiling Research," Redmond, August 2004.

20. *Infrastructure 2004: NSF CISE/EIA RI and MII PI's Workshop, Panelist*: "Research Challenges in Programming Languages: From Agendas To Impact," Snowbird, Utah, July 2004.
21. *University of Maryland*, College Park, "Enabling the Design of Compilers and Architectures for Emerging Applications," June 2004.
22. *University of California*, Irvine, Center for Embedded Computer Systems, "Frequent Value Locality and its Applications," May 2004.
23. *Arizona State University*, Tempe, Arizona, **CEINT Distinguished Seminar Series Speaker**, "Frequent Value Locality and its Applications," April 2004.
24. *Florida State University*, Tallahassee, FL, "Precise Dynamic Program Slicing Algorithms," April 2004.
25. *Intel Corporation*, Microcomputer Research Lab, Santa Clara, California, "Compiler and Architectural Support for Embedded Processors," March 2003.
26. *Penn State University*, State College, Pennsylvania, "Supporting Bit Section Addressing for Embedded Applications," December 2002.
27. *Purdue University*, West Lafayette, Indiana, "Supporting Bit Section Addressing for Embedded Applications," December 2002.
28. *Georgia Tech*, Atlanta, Georgia, "Architectural and Compiler Support for Performance Optimization Under Limited Power and Memory Resources," November 2002.
29. *Univ. of Texas at Austin*, Texas, "Frequent Value Locality and its Applications," Feb. 2002.
30. *Intel Corporation*, Microcomputer Research Lab, Santa Clara, California, "Frequent Values and their Applications," August 2001.
31. *Intel Corporation*, Microcomputer Research Lab, Santa Clara, California, "Optimizing Static Power Dissipation by Functional Units," August 2001.
32. *University of Alberta*, Edmonton, Canada, **Distinguished Lecture Series Speaker**, "Frequent Value Locality and its Applications," June 2001.
33. *University of Nevada at Reno*, Reno, Nevada, **IEEE Distinguished Speaker**, "Frequent Value Locality and its Applications," April 2001.
34. *Compaq*, Marlborough, MA, "Frequent Value Locality and its Applications," November 2000.
35. *Lucent Technologies*, Allentown, PA, "Path Sensitive Code Optimizations," June 1999.
36. *Georgia Tech*, Atlanta, Georgia, "Path Sensitive Code Optimizations," May 1999.
37. *Univ. of Maryland*, College Park, Maryland, "Path Sensitive Code Optimizations," April 1999.
38. *The Univ. of Arizona*, Tucson, Arizona, "Path Sensitive Code Optimizations," March 1999.
39. *Univ. of California, Los Angeles*, California, "Path Sensitive Code Optimizations," Jan. 1999.
40. *Florida State University*, Tallahassee, FL, "Path Sensitive Code Optimizations," Jan. 1999.
41. *IBM T.J. Watson Research Center*, Hawthorne, NY, "Profile Guided Redundancy and Dead Code Elimination," October 1998.
42. *Hewlett-Packard Labs*, Palo Alto, CA, "Path Profile Guided PRE and PDE," July 1997.
43. *Intel Seminar*, Santa Clara, CA, "A Demand-driven Framework for Interprocedural Data Flow Analysis," December 1996.
44. *Intel University Research Forum*, Santa Clara, CA, "Analysis and Optimization in an ILP Environment," November 1996.

45. *Hewlett-Packard Laboratories*, Palo Alto, CA, "Array Data Flow Analysis for Load-Store Optimizations in Superscalar Architectures," July 1995.
46. *Intel Corporation*, Santa Clara, CA, "Array Data Flow Analysis for Load-Store Optimizations in Superscalar Architectures," July 1995.
47. *Tartan, Inc.*, Pittsburgh, PA, "Demand-Driven Computation of Interprocedural Data Flow," June 1995.
48. *Tartan, Inc.*, Pittsburgh, PA, "Array Data Flow Analysis for Load-Store Optimizations in Superscalar Architectures," April 1995.
49. *Panelist*: "Program Transformations and Analysis for Real-Time Systems," *ACM SIGPLAN Workshop on Language, Compiler, and Tool Support for Real-Time Systems*, Orlando, FL, June 1994.
50. *Clemson University*, Clemson, South Carolina, "SPMD Execution of Programs on Distributed-Memory Machines," October 1993.
51. *Carnegie Mellon University*, Pittsburgh, PA, "A Practical Data Flow Framework for Array Reference Analysis and its Use in Optimizations," May 1993.
52. *University of Delaware*, Newark, Delaware, "SPMD Execution of Programs on Distributed-Memory Machines," December 1992.
53. *West Virginia University*, Morgantown, WV, "SPMD Execution of Programs on Distributed-Memory Machines," December 1992.
54. *NASA Ames Research Center*, Moffett Field, CA, "SPMD Execution of Programs on Distributed-Memory Machines," April 1992.
55. *IBM T.J. Watson Research Center*, Hawthorne, New York, "Fine-Grained Parallel Processing," April 1990.

PhDs In Progress

- (Expected 2019) Arash Alavi;
- (Started Spring 2015) Bryan Duane Rowe II; (Fall 2015) Gurneet Kaur; (Fall 2016) Abbas Mazloumi and Chengshuo (Bruce) Xu; (Fall 2017) Xiaolin Jiang.

PhDs Completed

1. Zachary Benavides, *Declarative Profiling for Parallel Systems*, September 2018. *Software Engineer, PushFor* (Current).
2. Hongbo Li, *Pre- and Post-Deployment Dynamic Bug Detection Techniques for MPI Programs*, September 2018. *Research Engineer II, TuSimple* (Current).
3. Keval Vora, *Exploiting Asynchrony for Performance and Fault Tolerance in Distributed Graph Processing*, completed June 2017. *Assistant Professor, Simon Fraser University* (Current).
4. Farzad Khorasani, *High Performance Vertex-Centric Graph Analytics on GPUs*, completed September 2016. *Senior Machine Learning Scientist, Tesla, Palo Alto, CA* (Current).
5. Vineet Singh, *User Assisted Data Structure Debugging and Verification*, completed September 2016. *Memory & Storage Tools Software Engineer, Intel, Hillsboro, OR* (Current).
6. Amlan Kusum, *Adapting Data Representations for Optimizing Data-Intensive Applications*, completed September 2016. *Member Technical Staff, Oracle, Denver, CO* (Current).
7. Bo Zhou, *Extracting Actionable Information From Bug Reports*, completed August 2016. *Java Engineer, WANdisco Inc., San Ramon, CA* (Current).

8. Sai Charan Koduru, *Size Oblivious Programming of Clusters for Irregular Parallelism*, completed September 2015. *Software Engineer, Microsoft, Redmond, WA* (Current).
9. Yan Wang, *Dynamic Analysis Techniques for Effective and Efficient Debugging*, completed August 2014. *Software Engineer, Google, Mountain View, CA* (Current).
10. Changhui Lin, *Imposing Minimal Memory Ordering on Multiprocessors*, completed August 2013. *Software Engineer, Google, Mountain View, CA* (Current).
11. Min Feng, *The SpiceC Parallel Programming System*, completed August 2012. *Research Staff Member, NEC Labs, Princeton, NJ* (Current).
12. Kishore Kumar Pusukuri, *Runtime Support for Exploiting Multicore Systems*, completed August 2012. *Staff Software Engineer, NetApp, Sunnyvale, CA* (Current).
13. Chen Tian, *Speculative Parallelization on Multicore Processors*, completed May 2010. *Principal Researcher, Huawei R&D Center, Santa Clara, CA* (Current).
14. Vijayanand Nagarajan, *IMPRESS: Improving Multicore Performance and Reliability via Efficient Support for Software Monitoring*, completed August 2009. *Associate Professor, University of Edinburgh, Edinburgh, UK* (Current).
15. Dennis Jeffrey, *Dynamic State Alteration Techniques for Automatically Locating Software Errors*, completed August 2009. *Senior Software Engineer in Test, Google, Mountain View, CA* (Current).
16. Sriraman Tallam, *Fault Location and Avoidance in Long-Running Multithreaded Applications*, completed October 2007. *Staff Engineer, Google, Mountain View, CA* (Current).
17. Xiangyu Zhang, *Fault Location Via Precise Dynamic Slicing*, completed September 2006. **Recipient of SIGPLAN Outstanding Doctoral Dissertation Award**, 2006. **NSF CAREER Award**, 2009. *Full Professor, Purdue University* (Current).
18. Bengu Li, *Efficient Handling of Narrow Width and Streaming Data in Embedded Applications*, completed May 2006. *Software Engineer, Tableau Software, Seattle* (Current).
19. Arvind Krishnaswamy, *Microarchitectural and Compiler Techniques for Dual-Width ISA Processors*, completed May 2006. *Senior Staff Engineer, Qualcomm, San Jose, CA* (Current).
20. Jun Yang, *Frequent Value Locality and its Application to Energy Efficient Memory Design*, completed September 2002. **NSF CAREER Award**, 2008. *Associate Professor, Univ. of Pittsburgh, PA* (Current).
21. Youtao Zhang, *The Design and Implementation of Compression Techniques for Profile Guided Compilation*, completed August 2002. **NSF CAREER Award**, 2005. *Associate Professor, Univ. of Pittsburgh, PA* (Current).
22. Clara Jaramillo, *Source Level Debugging Techniques and Tools for Optimized Code*, completed August 2000. *Chatam College, Pittsburgh, PA* (First Employment).
23. Ras Bodik, *Path and Value Sensitive Code Optimizations*, completed November 1999. **Recipient of SIGPLAN Outstanding Doctoral Dissertation Award**, 2001. **NSF CAREER Award**, 2001. *Full Professor, Univ. of Washington, Seattle* (Current).
24. Soner Onder, *Scalable Superscalar Processor Design*, completed July 1999. **NSF CAREER Award**, 2004. *Full Professor, Michigan Tech. University* (Current).
25. Xin Yuan, *Dynamic and Compiled Communication in Optical Time-Division-Multiplexed Point-to-Point Networks*, completed August 1998. *Full Professor and Department Chair, Florida State University* (Current).
26. Jodi Tims, *Integrating Automatic Data Distribution and Communication Optimization*, completed July 1998. *Full Professor and Department Chair, Baldwin Wallace College, Ohio* (Current).

27. Wanqing Wu, *On-line Avoidance of the Intrusive Effects of Monitoring of Distributed Applications*, completed July 1998. SAP Labs, Palo Alto, CA (Current).
28. Tia Watts, *MIST: An Approach to Integrating Restructuring Transformations and Multiple Scheduling Techniques*, completed December 1997. Full Professor, Sonoma State University, CA (Current).
29. David Berson, *Unification of Register Allocation and Instruction Scheduling in Compilers for Fine-Grain Parallel Architectures*, completed November 1996. Senior Compiler Engineer, NVIDIA, Portland (Current).
30. Evelyn Duesterwald, *A Demand Driven Approach for Efficient Interprocedural Data Flow Analysis*, completed July 1996.
ACM Distinguished Scientist, 2010. Senior Manager, IBM Research, New York (Current).
31. Chun Gong, *Fault Tolerant Computing on Distributed-Memory Systems: A Compiler Assisted Approach*, completed September 1995. Microsoft Corporation, WA (First Employment).

MS, UG, HS Student Supervision

1. (UG) Shawn Lee, *Efficient Parallel Sudoku Solver via Thread Management & Data Sharing Methods*, June 2017.
2. (UG) Andy Thio, *High Performance Parallel Sokoban Solver*, June 2017.
3. (HS) Jason Lai, Alta Loma High School, Rancho Cucamonga, Summer 2016.
4. (MS) Bin Wu, *Distributed Out-of-Core Graph Processing*, August 2015.
5. (UG) Sihan He, *TIGRAPH - A Tiny Graph Processing System*, June 2015.
6. (UG) Zhongqi Wang, *TIGRAPH - A Tiny Graph Processing System*, June 2015.
7. (MS) Bryan Duane Rowe II, *An Evaluation of Graph Processing Frameworks*, February 2015.
8. (UG) Joshua Giem, *Hybrid Parallel/Serial Loseless Data Compression on a GPU*, June 2014.
9. (MS) Pengcheng Zhao, *Reducing the Overhead of Dynamic Slicing*, August 2013.
10. (MS) Anton Jouline, *Dynamic Dispatching in Java Programs*, December 1999.
11. (MS) Jun Xu, *Implementation of Branch Sequence Prediction Techniques*, December 1998.
12. (MS) Aston AuYeung, *Extending UPFAST to Support VLIW Architectures*, August 1998.
13. (MS) Vishal Jain, *An Approach for Monitoring Intrusion Removal in Real-Time Systems*, 1997.
14. (MS) Philip Kamp, *Language and Compile-time Analysis Support for Dynamic Data Structures*, December 1995.
15. (MS) Xin Yuan, *Timestamp-based Selective Invalidation Scheme for Multiprocessor Cache Coherence*, August 1995.
16. (MS) Meena Krishnan, *Implementation of Array Data Flow Analysis in the PDGCC Compiler*, December 1994.
17. (MS) Wanqing Wu, *A Simulator for the PDGCC Compiler*, December 1994.
18. (MS) Ed Kuzemchak, *Automatic Test Generation for Testing Ada Compilers*, December 1994.
19. (MS) Ras Bodik, *Optimal Placement of Load-Store Operations for Array Accesses in Loops*, December 1994.

20. (MS) Kishore Karnam, *Automatic Distribution of Data on Distributed Memory Machines*, April 1994.
21. (MS) Radha Sivaramakrishnan, *Static Analysis of Distributed Memory Programs*, Dec. 1993.
22. (MS) Michael Bigrigg, *An Integrated Database Programming Environment for Parallel Applications*, August 1993.
23. (MS) Padmavathi Vallabhaneni, *Analysis and Transformation of Programs for SPMD execution on Distributed-Memory Multiprocessors*, December 1992.
24. (MS) Sunah Lee, *Executing Loops on a Fine-Grained MIMD Architecture*, August 1991.
25. (MS) Robert Kramer, *The Combining DAG: A Technique for Parallel Data Flow Analysis*, 1991.

DISSERTATION COMMITTEE MEMBER

UCR, CSE Department: Prerna Budhkar (2018); Kenneth O'Neal (2018); Yongjian Hu (2017); Panruo Wu (2016); Mehmet E. Belviranli (2016); Tanzirul Azim (2016); Mohammad Shokoohi-Yekta (2015); Dung Vu (2014); Teresa Davies (2014); Pamela Bhattacharya (2012); Guang-deng Liao (2011); Danhua Guo (2010); Min Wan (2008).

Georgia Tech., College of Computing: Xiaotong Zhuang (2006).

University of Arizona, ECE Dept.: Haibo Wang (2002); Daler Rakhmatov (2002).

Univ. of Pittsburgh, CS Dept.: Atif Memon (2001); Chuck Salisbury (1998); Chyi-Ren Dow (1994).

Carnegie Mellon University, CS Dept.: Chris Newburn (1997); Herman Schmit (1995).

New Jersey Institute of Technology, CS Dept.: Mohamed Younis (1996).

TEACHING EXPERIENCE

University of California, Riverside

CS 152: *Compiler Design* – Fall'08; Winter'10,'11,'12,'13,'14,'15,'16,'17,'18.

CS 203A: *Advanced Computer Architecture* – Winter'09.

CS 206: *Testing and Verification Techniques in Software Engineering* – Fall'09,'11,'12,'15.

CS 201: *Compiler Construction* – Winter'08; Spring'09,'10,'11,'12,'13,'14,'15,'16,'18; Fall'16,'18.

CS 260: Seminar: *Parallel Computing* – Spring'15.

CS 260: Seminar: *Multicore Systems* – Winter'11.

CS 260: Seminar: *Advanced Execution Systems for Reliable High-Perf. Computing* – Spring'08.

CS 270: *Special Topics in Advanced CS* – Spring'09,'17; Winter'10,'12,'13,'14,'16; Fall'18.

The University of Arizona

CSc 453: *Compilers and System Software*, Fall'99,'03.

CSc 553: *Principles of Compilation*, Spring'01,'02,'05,'07.

CSc 576: *Computer Architecture*, Fall'00,'01,'02,'03,'04.

CSc 620: *Microarchitecture and Compiler Support for Instruction Level Parallelism*, Spring'00.

CSc 620: *Embedded Systems*, Fall'02.

CSc 620: *Advanced Execution Systems for Reliable Computing*, Fall'06.

University of Pittsburgh

CS2210: *Compiler Design*, Fall'91,'92,'93,'94,'95,'97.
CS2212: *Advanced Compiler Design*, Winter'93,'94,'95.
CS2230: *Compiling Techniques for Parallel Systems*, Fall'93, Winter'96.
CS3210: *Advanced Topics in Programming Languages*, Winter'98,'99.
CS3220: *Seminar on Fine-Grained Parallel Processing Systems*, Winter'91.
CS1622: *Compiler Design*, Winter'91-96, Winter'98,'99.
CS1621: *Structure of Programming Languages*, Fall'90.
CS1520: *Programming Languages*, Fall'98.
CS0441: *Discrete Structures for Computer Science*, Winter'92.

UNIVERSITY SERVICE

University of California, Riverside

University Committee on Academic Personnel (UCAP), September 1, 2017 – August 30, 2018.
UCR Executive Council, September 1, 2018 – August 30, 2019.
UCR Committee on Academic Personnel (CAP), September 1, 2016 – August 30, 2019:
 Member 09/2016 – 08/2017;
 Vice-Chair 09/2017 – 08/2018;
 Chair 09/2018 – 08/2019.
UCR Grievance Consultation Panel (GCP), September 1, 2016 – August 30, 2019.
UCR Privelage and Tenure Committee (P&T), 2011 – 2013.
UCMEXUS Review Panel, 2012.
UC Discovery Review Panel, 2011.
Chair, Research Committee, Bourns College of Engineering Retreat, 2008.
Retreat Oversight Committee, Bourns College of Engineering, 2008 – 2009.
Chair, CSE Recruiting Committee, 2012 – 2014.
CSE Recruiting Committee, 2008 – 2012, 2015.
Chair, CEN Strategic Plan Committee, Fall 2018.
CEN Recruiting Committee, 2013 – 2015.
Graduate Admissions Committee, 2010 – 2012.
Graduate Program, 2015 – 2018.
Graduate Advisory Committee, 2015.
Executive Committee, CSE Department, 2007 – present.
University and Department Level AdHoc Committees for Peer Evaluations, 2007 – present.
Research Committee, 2007 – 2008.
Resource/Publicity Committee, 2008 – 2009.

The University of Arizona

Self-Study Team for Academic Program Review, *Member*, 2006 – 2007

Advisory Committee, *Member Elected by the Faculty*, 2006 – 2007.
Five Year Review Committee of Department Head, *Member Appointed by the Dean*, 2003.
Steering Committee, Research Infrastructure Grant: **Chair**, 2003-2005; *Member*, 2001 – 2002.
Graduate Admissions Committee: **Chair**, 2000 – 05/2005, 09/2006 – 2007; and *Member*, 1999.
Graduate Affairs Committee, *Member*, 2006 – 2007.
Space Planning Committee, *Member*, 2004.
Colloquium Czar, 2001 – 2002.
Human Subjects Review Committee, *Chair*, 2003 – 2005.
Promotion and Tenure Committee, *Member*, 1999 – 2001 and 2002 – 2005.
PhD Qualifiers Committee, 2001 – 2002.

University of Pittsburgh

Computer Engineering Program Proposal Committee, *Member*, 1995.
Committee on the University of Pittsburgh's Presentation on the Internet, 1995.
Faculty of Arts and Sciences Tenure Review Committees, **Chair & Member**, 1998 & 1999.
Faculty of Arts and Sciences Tenure Council, *Member*, 1994, 1995 and 1998
Faculty Recruiting Committee, *Member*, 1990 – 1991.
Graduate Programs and Exams Committee, *Member*, 1991 – 1993.
Graduate Admissions and Financial Aid Committee, *Member*, 1992 – 1993 and 1998 – 1999.
TA/TF Training and Evaluation Committee, *Member*, 1994 – 1995.
Computing and Communications Committee, *Member*, 1994 – 1999.
Web Administrator for the Computer Science Department, 1994 – 1999