A Low-cost Field-Programmable Pin- Constrained Digital Microfluidic Biochip

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Abstract—This paper introduces a field-programmable pin-constrained digital microfluidic biochip (FPPC-DMFB), which offers general-purpose assay execution at a lower cost than general-purpose direct addressing DMFBs and highly optimized application-specific pin-constrained DMFBs. The key cost driver for is the number of printed circuit board (PCB) layers, onto which the device is mounted; we demonstrate a scalable single-layer PCB wiring scheme for several FPPC-DMFB variations, for PCB technology with orthogonal routing capacity of at least three; for PCB technology with orthogonal capacity of two, more PCB layers are required, but the FPPC-DMFB retains its cost advantage. These results offer new insights on the relationship between PCB layer count, pin count, and cost. Additionally, to reduce the execution time of assays on the FPPC-DMFB, we present efficient algorithms for droplet routing, with and without contamination removal via wash droplets.

Index Terms—Digital Microfluidic Biochip (DMFB), Pin-constrained DMFB, PCB escape routing

I. INTRODUCTION

A field-programmable, pin-constrained digital microfluidic biochip (FPPC-DMFB), can execute any assay (biochemical protocol) after the device has been manufactured [12]. Prior general-purpose DMFBs were based on direct addressing, which provides independent control over each electrode in the device, at the cost of a high number of control pins, which requires expensive multi-layer printed circuit boards (PCBs). Prior pin-constrained DMFBs, allow each control pin to drive multiple electrodes [36], reducing the number of control pins and PCB layers; however, they have all been application-specific [9][18][19][20][21][23][24][25][28][36][38][40][41] [42], which limits their usability. In contrast, the FPPC-DMFB is general purpose and can be implemented in one PCB layer. We demonstrate that the FPPC-DMFB is cheaper than direct addressing and prior application-specific pin-constrained DMFBs. Our results and analysis provide new understanding into the relationship between pin count, layer count, and the actual cost of the chip. We also demonstrate efficient droplet routing algorithms for the FPPC-DMFB, and establish the overhead of contamination removal via wash droplet routing.

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2) Background: High-level Assay Synthesis

**Synthesis** is the process that maps a biochemical reaction (an *assay*), onto a DMFB, as shown in Fig. 3. An assay is specified as a directed acyclic graph (DAG), where vertices represent fluidic operations (e.g. mix, split, etc.) and edges represent precedence and droplet transfer between operations. The DAG in Fig. 3 depicts a simple assay that inputs two droplets, mixes them, and outputs the resulting droplet.

The first step of synthesis is **scheduling**, which assigns start and stop time to each operation (e.g., the mix operation, *M1*), executes from time steps 1 to 4 in Fig. 3). Next, the **placement** step decides which DMFB locations perform each operation. For dispense (input) operations, a reservoir containing the appropriate fluid is chosen. “Reconfigurable” operations such as mixing and splitting can be performed anywhere on the chip; for example, in Fig. 3, the mix operation *M1* is placed in the 2x2 array of cells in the top-right corner of the DMFB; however, *M1* could be placed in any unoccupied 2x2 array of cells on the DMFB. The array of cells that denotes the location of an operation is called a **module**. Lastly, the **routing** step computes paths for droplet transport between operations that have been scheduled and placed. The router produces a list of electrodes to activate during each droplet actuation cycle, i.e., the time it takes to move a droplet from one electrode to the next. While computing droplet routes, the router must ensure that droplets do not interfere with one another while traversing the DMFB array [13][14][35]; to prevent droplets from accidental collisions, the router creates an interference region around a stationary droplet at the beginning of a droplet actuation cycle, as seen in Fig. 4(a). As the droplet moves to an adjacent electrode, the interference region stretches to include all the electrodes surrounding the droplet’s initial and final electrode (Fig. 4(b)). Collisions are prevented by ensuring that no droplet enters the interference region of any other droplet (unless they are about to merge).

3) Background: Pin Mapping and PCB Wire Routing

**Synthesis** typically targets an existing DMFB that has been designed and fabricated; alternatively, it can be coupled with pin mapping and wire routing phases to produce an optimized application-specific chip. The default pin mapper instantiates a **direct addressing DMFB**, in which each electrode is wired to an external electrical control pin, as shown in Fig. 5(a)). Direct addressable DMFBs offer the most flexibility in terms of droplet coordination; however, the large number of control pins can increase the two-dimensional area, and thus cost, of the PCB on which the DMFB is mounted. (Fig. 6(a)).

Pin mapping converts a direct-addressing DMFB into a **pin-constrained DMFB** by tethering multiple electrodes together so that a single control pin can activate them (Fig. 5(b)). In Fig. 3, the pin-mapper removes the 10 non-used electrodes and connects the remaining ones in to reduce the number of control pins from 15 to 7. Reducing the number of control pins reduces the overall cost of the device [24][36][38][40][42].

**PCB** wire routing establishes physical connections within the PCB from each external control input to the electrode(s) that it drives, as determined by the pin mapper. In Fig. 1(b), electrodes reside on the lower substrate of the DMFB, while wire routing is performed within the PCB (shown in green in Fig. 3 and Fig. 6(b)).** PCB** wire routing for pin-constrained DMFBs is a multi-terminal variant of the PCB escape routing problem [7][26][37]. Effective escape routers can reduce the number of PCB layers, and thus the overall cost of the device.

Past work on this topic has focused on the number of control pins and/or the number of PCB layers as a proxy for PCB cost. In this work, we estimate the actual cost of the PCB layout in dollars and discuss the various tradeoffs involved.
B. Contribution

The FPPC-DMFB is the first pin-constrained DMFB that is also general-purpose [12]. This paper introduces the FPPC-DMFB pin assignment scheme, describes a synthesis flow that targets it, and presents a PCB wire routing solution that minimizes its overall cost. Our results establish the feasibility of concurrent assay operations and droplet transport on the FPPC-DMFB, quantify the performance overhead of cross-contamination elimination via wash droplet routing, and show that a PCB designed for an optimized FPPC-DMFB can be significantly cheaper than a PCB designed for both direct-addressing and application-specific pin-constrained DMFBs.

II. RELATED WORK

Early pin mappers tried to minimize the pin count, but did not consider the impact of pin count reduction on the number of PCB layers. Under array partitioning [36], different groups of control pins are assigned to each partition, reducing or eliminating interferences among droplets that are transported concurrently. Broadcast electrode addressing [42] examines the electrode activation sequence produced by a synthesis tool and identifies electrodes that can share a control input. Luo and Chakrabarty [25] introduced a pin assignment scheme that facilitates interference-free and deadlock-free concurrent transport of up to two droplets. Several other papers optimize pin assignment in conjunction with other synthesis tasks, especially droplet routing [9][18][23][24][28][41].

Escape routing for PCBs routes known pins in a large array to the array perimeter [26][37]. For pin-constrained DMFBs, the escape routing problem must accommodate multi-terminal nets for control inputs that drive multiple electrodes. One paper has been published that focuses explicitly on escape routing for DMFBs [7], while another optimizes the PCB layout for multiple DMFBs that execute the same protocol concurrently in a lock-step [32]. Several papers have also been published that optimize pin assignment in conjunction with escape routing [19][20][21][38]; they optimize application-specific, not general-purpose pin-constrained DMFBs.

The FPPC-DMFB is a pin-constrained virtual topology [11][13][14], which segregates the DMFB surface area into modules that perform assay operations (mixing, splitting, storage, detection, etc.) and a network of streets that transport droplets between modules and I/O reservoirs. In a direct-addressing chip, virtual topologies limit the flexibility and reconfigurability of the device in order to facilitate fast online synthesis algorithms, which can respond to sensory feedback provided by the device in real-time [13][14]. Pin-constrained DMFBs exhibit limited flexibility and reconfigurability; imposing a virtual topology to achieve general-purpose operation is a favorable innovation [12].

Chang et al. [8] introduced a pin-constrained DMFB that shares some similarities with the FPPC-DMFB proposed here. Their device does not account for some of the finer details of module/device synchronization and I/O addressed in this paper (e.g., the ability to independently load/unload droplets into modules). It is also unclear if the layout and wiring solution is scalable to larger devices. In contrast, this paper presents a design variation of the FPPC-DMFB which can be routed in one PCB layer, and can scale to arbitrary numbers of operational and storage modules.

III. PIN ASSIGNMENT

The FPPC-DMFB employs a pin assignment scheme that enables all of the basic assay operations (Fig. 2) to execute in a conflict-free manner. Fig. 7 shows two similar, but different, 10x16 FPPC-DMFB layouts. For simplicity we first focus on the pin-optimized version in Fig. 7(a) to show the general characteristics of our FPPC-DMFB design.

Similar to virtual topologies [11][13][14], the FPPC-DMFB reserves specific regions for assay operations and others for routing. The FPPC-DMFB contains a vertical column of mixing modules on the left (blue/orange electrodes, Pins 10-20) and a vertical column of modules on the right (orange electrodes, Pins 31-36) that perform splitting, storage, and detection (which requires an external detector affixed above the module); we call these modules SSD modules.

White electrodes define droplet routing regions, which ensure full connectivity between all modules. I/O reservoirs can be placed anywhere along the top or bottom of the chip, as seen in Fig. 7. The green electrodes, Pins 21-30, allow droplets to enter/exit each module. An interference region (gray) surrounds each module to isolate droplets within it from droplets in the routing region or adjacent modules; these regions are not functional and do not contain electrodes.
The layout is designed for operation concurrency; mix and SSD modules can execute different operations that may start and stop at any time-step (i.e., droplets may enter/exit modules while other modules continue operating). The architecture is scalable and can be vertically lengthened or shortened to produce a DMFB with any desired number of modules.

A. DMFB Operations and Synchronization

1) Droplet Transport

The FPPC-DMFB facilitates droplet transfer between horizontal and vertical transport buses. Routable paths exist between all modules and I/O reservoirs on the chip’s perimeter. Chips of arbitrary height can be instantiated without altering the wire-routing pattern (see Section IV.B). The mix and SSD module-hold electrodes (Fig. 7(a), Pins 17-20 and Pins 31-36, respectively) remain active during routing to ensure that droplets within the modules do not drift.

Pin-optimized FPPC-DMFB: Fig. 8 shows that at least 3 pins are required to successfully transport a droplet along a straight path; this is called a 3-phase transport bus [33]. In Fig. 7(a), Pins 1-3 and Pins 7-9 control two horizontal buses; Pins 4-6 drive a vertical transport bus at the center of the array.

Route-optimized FPPC-DMFB: Replacing 3-phase transport buses with direct addressing buses rectifies the situation in Fig. 9. The route-optimized design increases the control pin count by 25 to facilitate concurrent droplet routing; the pin assignment for mixing and SSD modules is unchanged.

2) Droplet Dispensing and Output

I/O reservoirs are attached to the top and bottom horizontal transport buses, and have individually addressable electrodes, (red in Fig. 7) to allow droplets to enter/exit the chip.

3) Merging/Mixing

Fig. 10(a) shows a droplet (D2) entering and exiting a mixing module (M2) without conflicting with droplets in other modules (D1, D3). On top, D2 reaches the electrode adjacent to the mixing module (M2); D1 is in mixing module M1 and D3 is stored in SSD module SSD1. All SSD module electrodes are activated (Pins 24-26) to hold the stored droplets in place during mixing module I/O. Activating Pin 20 (M2’s I/O cell) moves D2 adjacent to M2. Activating Pin 16 draws D2 into M2, while transporting D1 to an adjacent cell within M1. Next, all mixer hold cells (Pins 17 and 18) move D1 and D2 to identical positions within M1 and M2. The electrode sequence is reversed when a droplet exits a mixing module.
Two droplets must merge before mixing, as shown in Fig. 11: droplet D4 merges with droplet D2 in M2 forming a new droplet, D5 (with twice the volume) and re-sync with any other droplets in mix modules (i.e., D1 in M1).

M1 and M2 perform concurrent synchronized mixing by activating Pins 10-16, in sequence, starting with Pin 15 and continuing counterclockwise (i.e., Pin 15, 14, 11, 12, 13, 16), followed by Pin 17 and 18 together. Mixing can pause if one droplet needs to enter or exit any mixing module.

4) Storage, Detection, and Splitting
SSD modules perform storage and detection (if equipped with an external detector). Both operations require a droplet to enter an SSD module and remain in place. Fig. 10(b) illustrates a droplet entering/exiting an SSD module (SSD3) without affecting droplets in other modules. All SSD hold electrodes are activated, except for SSD3’s, which allows D2 to enter. SSD3’s I/O electrode is then activated, followed by its hold electrode, to complete the entrance. This sequence is reversed to let a droplet exit an SSD module.

Fig. 12(a)-(c) illustrates splitting. Droplet D2, which will be split, starts on a vertical transport bus by an SSD module’s I/O cell; this cell remains activated throughout the split. Next, the I/O cell is activated, stretching D2. Then the SSD module’s hold cell is activated and the I/O cell is deactivated, splitting D2 between the hold cell (D2), and the bus (D4). D4 can then be routed to an available SSD module for storage (Fig. 12(d)).

IV. HARDWARE LAYOUT OPTIMIZATION

A. Problem Formulation
This section introduces a deterministic and scalable co-optimized pin assignment and single-layer PCB wire routing solution for the FPPC-DMFB. The input is an architecture description, which includes the XY-dimensions of the chip, locations of I/O ports on the periphery of the horizontal buses, PCB feature sizes and a flag that indicates whether the user wants a pin-optimized or route-optimized FPPC-DMFB. The output is a programmable pin-mapping solution, which fits the user-provided dimensions, and a valid single-layer PCB wire routing solution, which adheres to the pin mapping solution.
B. Co-optimizing Pin Assignment and Wire Routing

As a motivating example, consider a pin assignment for a pin-constrained 15x15 assay-specific DMFB designed for the PCR assay [42]. Fig. 13(a) shows a 14-pin layout and highlights the wire routing solution for Pin 1; Pin 1 drives 9 electrodes, many of which are on the perimeter of the chip. The wire routing solution for this one pin effectively blocks the ability to route additional wires into the chip on the same PCB layer. Fig. 13(b) shows a complete wire routing solution for all 14 pins; a total of four PCB layers are required.

Fig. 15. The single-layer wire-routing solutions for the enhanced FPPC-DMFB designs in this paper for the (a) pin-optimized version (Fig. 7(a)) and (b) route-optimized pin-mapping (Fig. 7(b)).

Fig. 14 presents two pin mapping and wire routing solutions for two FPPC-DMFB variants. Fig. 14(a) presents the original pin mapping architecture [12], and Fig. 14(b) shows the wire-routing solution obtained by the negotiated-congestion escape router [26]. This particular variant has three vertical buses (as opposed to the one central vertical bus shown in Fig. 7). Four PCB layers are required for routing, as shown in Fig. 14(b).

Fig. 14(c-d) depicts two of these four wire-routing layers. Wires that connect to electrodes on the 3-phase buses must span the entire array, essentially blocking the ability of other wires to escape from the perimeter on the same PCB layer. To eliminate this problem for the pin-optimized version, we removed the two side buses and use separate three-phase buses (Pins 1-3, 4-6, 7-9) to control the three remaining buses, as shown in Fig. 7(a). This yielded a single-PCB layer wire routing solution, shown in Fig. 15(a). The route-optimized version also removes the periphery vertical bus, but uses individually addressable electrodes, as seen in Fig. 7(b). Fig. 15(b) reveals the single-layer wire-routing solution, showing that the individually addressable bus electrodes are easily escapable and do not create large obstacles for other pins. We have implemented an algorithm to generate these escape routes for FPPC-DMFBs of varying vertical length.

Removing the left and right vertical buses may reduce the number of potential I/O locations; however, if extra I/O is required, the horizontal buses at the top and/or bottom can be extended; alternatively, mixing or SSD modules in the center of the chip could be replaced with an I/O reservoir attached to the central vertical bus. Another subtle detail is that an extra horizontal row is added between the top vertical bus and the topmost mixing and SSD modules; this extra space is needed to provide access for control wires that drive electrodes in the center of the chip to escape, as shown in Fig. 15.

The original design assumed that Pins 7-13 (see Fig. 14(a)) could be shared by an arbitrary number of mixing modules, regardless of the height of the chip; however, because of the independently controlled module hold and I/O pins (Pins 14-21 in Fig. 14(a)), there is not enough room to extend the shared pins indefinitely without introducing additional PCB layers to facilitate wire routing to these shared electrodes.
A. Problem Formulation

The input to the high-level synthesis stage is an architecture description (array dimensions, I/O location, pin assignment), and a DAG representing an assay. After scheduling, placing, and routing the DAG, the output is a valid electrode activation sequence that executes all steps of the assay on the device.

B. Scheduling

Schedulers targeting direct addressing DMFBs treat the device as being reconfigurable, where any operation other than I/O or detection can be performed anywhere. When targeting the FPPC-DMFB, the number of mixing and SSD modules impose a resource limit. We modified list scheduling [15][34] and path scheduling [16] to target the FPPC-DMFB.

Modules in direct-addressing DMFBs can perform mixing and storage, and may store multiple droplets. Schedulers targeting direct-addressing DMFBs may route stored droplets from one module to another in order to free up modules to perform other operations [15][16][30]. Since SSD modules store at most one droplet, a scheduler targeting the FPPC-DMFB can eliminate these unnecessary routing transfers.

The scheduler reserves one SSD module to address routing deadlocks, as explained later in Section D. Thus, in Fig. 7, only 5 of the 6 SSD modules are available for general use.

C. Placement/Binding

Similar to placement algorithms targeting direct-addressing virtual topologies [13][15], we reduce placement to a binding problem, which is solved using the left-edge algorithm [22]. Synthesis software targeting the FPPC-DMFB does not bind a split operation to a module, as the split yields two immediate storage operations (Fig. 17). Instead, the software binds the children to the SSD modules directly.

D. Droplet Routing

A routing sub-problem refers to the set of droplets that must be routed just before each time-step begins [35][39]. We refer to the routes that transport droplets between operations in the original assay specification as functional routes. Routes are computed one-at-a-time, ignoring, for the moment, other droplets that also need to be routed during the same time-step: (1) to route a droplet from an input reservoir to module, the router computes a deterministic path over the horizontal and vertical buses, and applies the appropriate module input sequence when the droplet arrives (Section III.A); (2) a similar approach is taken to route droplets from modules to output reservoirs; 3) module-to-module routing uses the vertical column in the center of the chip, applying appropriate input/output sequences at the start/end of the route.

V. HIGH-LEVEL SYNTHESIS

A. Problem Formulation

The input to the high-level synthesis stage is an architecture description (array dimensions, I/O location, pin assignment), and a DAG representing an assay. After scheduling, placing, and routing the DAG, the output is a valid electrode activation sequence that executes all steps of the assay on the device.

Fig. 16. The wire-routing model for the FPPC-DMFB (pin-optimized version shown) generalizes to an unlimited number of modules; each group of up to four mixing modules shares seven common pins as seen in FPPC-DMFBs with (a) eight mixing modules and (b) 5 mixing modules.

The solution is to limit the number of shared electrodes to groups of four continuous mixing modules (Fig. 15). For chips with more than four mixing modules (e.g., Fig. 16) the same layout and wiring pattern as in Fig. 15 is repeated. Fig. 16(a) shows two groups of four mixing modules, while Fig. 16(b) generalizes the scheme to an arbitrary number. This approach generalizes to the route-optimized design as well.

C. Escape Routing Details

The orthogonal capacity of a PCB is the number of wires that can route between two orthogonally adjacent electrodes. We have assumed an orthogonal capacity of 3 throughout this section [21][38]; this allows for a diagonal capacity of 6 (i.e., at most 6 wires can be routed between diagonally adjacent electrodes); ref. [37] provides more details on modeling these capacities. All escape routing results for architectures other than the FPPC-DMFB presented in this paper were obtained using an internally implemented multi-terminal variant of an escape routing algorithm based on negotiated congestion [26].
Dependencies and Deadlock: Routing deadlock occurs when one or more droplets wait for resources to become available that will never become free; for example, Fig. 18(a) shows a cyclic dependency involving two droplets. To break the cycle, one droplet (D3) is routed to an empty SSD module (SSD2), as shown in Fig. 18(b). In Fig. 18(c), the dependency is broken, but droplet D3 must wait for D1 to complete its route. The scheduler reserves one SSD module as a routing buffer to break any cyclic dependencies that may result from binding.

Wash Droplet Routing: A droplet traveling on a DMFB may leave residue behind that contaminates other droplets. Wash droplets may be dispatched to clean electrodes that have been contaminated by a previous droplet; a future droplet can then travel over the cleaned electrode without being contaminated.

In Fig. 19, operations Mix2 and Mix3 each demand two droplets to be routed to their assigned modules at time-step 10; Fig. 19 depicts these routes as R1-R4. Since R1 and R2 travel to the same destination to be merged, they cannot contaminate one another and no wash droplet is needed; the same is true for R3 and R4. Assume that R1 and R2 are routed first; if either R3 or R4 crosses over any of the same electrodes as R1 or R2, contamination could occur and must be prevented.

First, we designate dedicated wash fluid input and output ports on the top and bottom horizontal buses respectively. We then identify all operations starting at the given time-step (e.g., for time-step 10 in Fig. 19, Mix2 and Mix3). The first operation is examined and routes are generated to its assigned module (or output port) from all of its parents; without loss of generality, assume Mix2 is being examined, and thus, R1 and R2 are generated to transport droplets from the input reservoirs to Mix2’s mix module. Next, a wash droplet is generated and a route is computed to cover all of the electrodes covered by R1 and R2 on any of the transportation buses. Since the wash I/O ports are on opposite sides of the array, the entire vertical bus is cleaned each during each washing step. When considering Mix3, where routes are being cleaned that begin in a module (R3 begins in a SSD module, R4 begins in a mix module), the wash droplet enters and cleans each source module on its way down the vertical bus, cleaning all contaminated electrodes in both transportation buses and modules.

Concurrent Routing: As discussed in Section III the pin-optimized FPPC-DMFB must employ sequential routing to prevent unintended droplet splitting and drifting. Thus, wash droplet routes are inserted and executed after each operation executes its parent routes. In contrast, the route-optimized FPPC-DMFB employs individually addressable buses, which facilitates concurrent functional and wash droplet routing.

Similar to prior work by Grissom and Brisk [14], the concurrent router compacts the sequential routing solution (in time) so that multiple droplets can route in parallel without inadvertently colliding. Their algorithm compacts droplet routes one-at-a-time, delaying the starting time of each route until a legal solution is obtained. In the worse case, the compacted solution ends up being sequential.

To incorporate wash droplets and the FPPC-DMFB’s virtual topology, several new compaction rules are introduced.

1.) No droplet may cross a contaminated electrode.
2.) Two mixing modules cannot be cleaned at the same time; a droplet may not enter or exit any mixing module while another is being cleaned.
3.) Two (or more) droplets may not simultaneously enter and exit two distinct mixing modules at the same time.

If any of these rules is broken during compaction, stalls are inserted at the beginning of the route until legality is obtained. To address Rule 1, a wash droplet must be routed before the current droplet can be compacted. Rules 2 and 3 are specific to the FPPC-DMFB’s shared mixing module pins (see Fig. 7). To illustrate Rule 2, Fig. 20(a) shows how a droplet entering a module during mixing may unintentionally split because of the simultaneous pin activations due to wash droplet traversal. Fig. 20(b) illustrates Rule 3: two droplets simultaneously entering and exiting mixing modules may inadvertently split.

Once all routes are compacted, we can reduce the length of the routing sub-problem. Typically, operations such as mixing are paused during the routing portion of an assay to allow all droplets to reach their destination and sync [13][14]; however, if all droplets still en route to their destinations are traveling to output reservoirs and are not on a mix electrode (shared, hold or I/O), then the next time-step may commence, overlapping a portion of the routing stage with an operational stage. The mix modules can start to activate their shared pins in a lockstep rotational pattern; these activations could interfere with any droplets concurrently exiting a mixing module, but not with droplets undergoing transportation on one of the buses.
VI. EXPERIMENTAL METHODOLOGY

A. Wire Routing Cost Analysis

Our experiments estimate the cost (in US dollars) of PCBs for different direct-addressing and pin-constrained DMFB architectures, along with several variants of the FPPC-DMFB. Prior work has reported pin-count and the number of PCB layers as a proxy for cost, but has not reported the actual costs. This makes it difficult to determine when it is profitable to increase the pin count if doing so reduces the number of PCB layers. Our experimental approach presents a more accurate picture of the tradeoffs involved here.

We use Advanced Circuits’ online instant quote feature to estimate the cost of each PCB [2]. We provide the PCB length and width and the number of wire-routing layers. Vias connect multiple layers, and thus it is necessary to specify the via size, along with the wire trace spacing and size, which dictates the thickness of wire traces and the minimum spacing between tracing. All other metrics are left at their default values. Wire-length does not directly affect the cost, as long as the PCB is routable without increasing its area by adding extra space.

We assume that all DMFBs are driven by an Atmega 1284 microcontroller with 32 general purpose I/Os (GPIOs) to address the DMFB array [3]. If a DMFB has 32 or fewer control pins, no additional circuitry is needed; shift registers are required to drive additional pins in excess of 32. Shift registers can be daisy chained to feed an arbitrary number of additional inputs using 4 microcontroller signals to control the shift register chain: the serial data input (SER), shift register clock input (SCK), storage register clock input (RCK) and the reset input (SCLR). We assume the Fairchild 74VHC595MTC 8-bit shift register [4], which can be purchased from Mouser for $0.14 per unit in quantities of 2,500 [6]. Equation (1) reports the number of shift registers required for a DMFB.

\[
\text{numShiftRegs} = \begin{cases} 
\frac{\text{numPins} - 28}{8}, & \text{numPins} > 32 \\
0, & \text{otherwise}
\end{cases}
\] (1)

The Atmega 1284 operates at 20MHz [3]; the droplet actuation frequency (i.e., the time it required to transport a droplet between two adjacent electrodes) of a typical DMFB is 100Hz [39]. With an estimate of 5 cycles per shift operation, the Atmega 1284 can load 400 pin values into the shift registers in 1% of the droplet actuation cycle, maintaining sufficient signal integrity for proper droplet transportation.

Equation (2) models the PCB wire routing cost as the sum of the PCB price estimate from Advanced Circuits and the shift registers to connect all pins. We do not include the cost of the microcontroller, which is constant, irrespective of the choice of DMFB. We do not consider the cost of circuitry to amplify the voltage produced by the microcontroller to levels appropriate to drive the DMFB. Typical actuation voltages are in the 50-70V range [29][31]; low voltage devices that operate at ~15V have also been reported [10][27].

\[
\text{CostWR} = \text{Cost}_{PCB} + \text{Cost}_{SR}
\] (2)

The wire-routing cost is a function of the number of PCB layers, the PCB area, and wire trace width, as shown in Equation (3). Assuming an orthogonal capacity of 3 or more, the FPPC-DMFB requires one PCB layer, as shown in Fig. 14(f) and Fig. 16. In all other cases, we use the negotiated congestion escape router [26] to determine the number of PCB layers that achieve a legal route. Using larger feature sizes tends to reduce the PCB cost estimate [2].

\[
\text{Cost}_{PCB}(\text{numLayers}, \text{width}_{PCB}, \text{height}_{PCB}, \text{width}_{F})
\] (3)

Equation (4) computes the orthogonal capacity according to the metrics in Table 1 and diagram in Fig. 21. With an electrode pitch of 2 mm, wire trace width and spacing of 0.007 in, in width of 0.014 in and in contact width of 0.024 in, we estimate the orthogonal capacity to be \(o_{cap} = 3.12 = 3\).

![Fig. 21. A top-down and cross-sectional view of a PCB showing dimensions for the electrode pitch (ELEC), via hole (V), via contact (VC), wire trace (T) and minimum wire trace spacing (VS) in a DMFB.](image)

![Fig. 22. The component layout for PCB size estimation. The electrode array is surrounded by a 0.5 inch perimeter of empty space. The PCB width is extended to add as many shift registers as necessary.](image)
assays used in their experiments (PCR, INVITRO, PROTEIN) or a multi-functional chip that is co-designed to perform all three of those assays (MULTI). The electrode layouts are identical for both of these works; only the pin-assignment is different. We also created directly addressable versions of the corresponding electrode layouts, entitled XXX_DA.

We denote the FPPC as FPPC_4_MODULE for the 4-mixer version shown in Fig. 14(e) and FPPC_8_MODULE for the 8-mixer version shown in Fig. 16(a). The routing-optimized FPPC-DMFB (Fig. 7(b)), with 4- and 8-mixers are named FPPC_4_DA_BUS and FPPC_8_DA_BUS respectively.

We also consider two direct addressing DMFBs that use the 4- and 8-mixer FPPC-DMFB electrode layouts in Fig. 14(e) and Fig. 16(a); these chips are named FPPC_4_DA and FPPC_8_DA, respectively. Lastly, we include results for three direct-addressing DMFBs having dimensions: of 15x15 (15x15_DA), 10x10 (10x10_DA), and 10x30 (10x30_DA).

PCB escape routing solutions for all FPPC-DMFBs, except for the directly addressable ones, were computed as described in Section IV.B (FPPC); all other DMFB wire routes were computed using a multi-terminal implementation of an escape router based on negotiated congestion [26]. If a pin’s wire net cannot be routed on a top-level layer, it is routed on a lower layer in its entirety using vias to connect the wire net to its corresponding electrodes and to the external driving pin.

B. PCB Layers & Orthogonal Capacity

We examine the relationship between orthogonal capacity, the number of control pins and the number of PCB layers. The right side of Table II shows the number of PCB layers required to route each DMFB as the orthogonal capacity varies from 2 to 10. The dark squares highlight the lowest orthogonal capacity that achieves the smallest number of layers for each benchmark: 16/21 ≤ 76% and 19/21 ≤ 90% of the benchmarks minimize the number of layers at orthogonal capacities of 3 or 4. For ZHAO XXX and LUO XXX, the minimum number of PCB layers ranges from 3 to 6.

As an example, consider ZHAO_PCR, which is shown in Fig. 13. This particular pin mapping requires long wires along the perimeter of the chip, which prevent other wires from escaping on the same PCB layer; thus, additional layers are necessary. Reducing the wire size to increase orthogonal capacity does not reduce the number of PCB layers; however, converting this chip to a direct-addressing design (XXX_DA) yields single-layer escape routing solutions for any orthogonal capacity, but increases the control pin count by 2x to 4.4x.

The FPPC-DMFBs shown in Table II can be routed in 1 or 2 PCB layers, even at the smallest orthogonal capacities. FPPC_4_MODULE’s pin count is comparable to ZHAO XXX and LUO XXX, indicating that the FPPC-DMFB offers the advantages of being both general-purpose and low cost.

C. Wire Routing Cost Analysis

We vary the electrode pitch (1, 2, 2.54 mm), and determine the parameters for each that minimize cost. We translate these results into PCB cost estimates for the DMFBs in Table II.
The left side shows various metrics used for the Advanced Circuit PCB cost estimator [2] and resultant orthogonal capacity (oCap). The right side provides corresponding price estimates from the Advanced Circuit PCB cost estimator for a 2"x2" PCB with varying numbers of layers; dark rows represent the selected metrics for each electrode pitch.

### Table III
**Price Estimations for Varying Numbers of Layers and Parameters of a 2"x2" PCB**

<table>
<thead>
<tr>
<th>Electrode Pitch (mm)</th>
<th>Advanced Circuit Metrics</th>
<th>2&quot; x 2&quot; Price (@ 2,500 QTY) with Varying Number of Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Trace Size/Space (in)</td>
<td>Via Size (in)</td>
</tr>
<tr>
<td>0.097</td>
<td>0.005 0.010 0.013</td>
<td>2</td>
</tr>
<tr>
<td>0.098</td>
<td>0.006 0.011 0.014</td>
<td>3</td>
</tr>
<tr>
<td>0.099</td>
<td>0.007 0.012 0.015</td>
<td>4</td>
</tr>
<tr>
<td>0.100</td>
<td>0.008 0.013 0.016</td>
<td>5</td>
</tr>
</tbody>
</table>

The right side shows various metrics used for the Advanced Circuit PCB cost estimator [2] and resultant orthogonal capacity (oCap). The right side provides corresponding price estimates from the Advanced Circuit PCB cost estimator for a 2"x2" PCB with varying numbers of layers; dark rows represent the selected metrics for each electrode pitch.

### Table IV
**Cost Estimates for 21 DMFBs with 1 mm Electrode Pitch and Orthogonal Capacity of 2**

<table>
<thead>
<tr>
<th>DMFB Details</th>
<th>Cost ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Board</strong></td>
</tr>
<tr>
<td>FFPC_4_MODULE</td>
<td>36 1 1.7638 1.6299 2</td>
</tr>
<tr>
<td>ZHAO_PCR</td>
<td>14 0 1.5906 1.5906 4</td>
</tr>
<tr>
<td>ZHAO_INVITRO</td>
<td>25 0 1.5906 1.5906 4</td>
</tr>
<tr>
<td>LUI_PROTEIN</td>
<td>27 0 1.5906 1.5906 4</td>
</tr>
<tr>
<td>LUI_PROCESS</td>
<td>21 0 1.5906 1.5906 4</td>
</tr>
<tr>
<td>ZHAO_MULTI</td>
<td>32 0 1.5906 1.5906 5</td>
</tr>
<tr>
<td>LUI_PCR</td>
<td>22 0 1.5906 1.5906 5</td>
</tr>
<tr>
<td>LUI_INVITRO</td>
<td>21 0 1.5906 1.5906 5</td>
</tr>
<tr>
<td>LUI_MULTI</td>
<td>27 0 1.5906 1.5906 6</td>
</tr>
<tr>
<td>PRODUC_D4</td>
<td>54 4 1.9606 1.9606 1</td>
</tr>
<tr>
<td>INVI_D2</td>
<td>59 4 1.9606 1.9606 1</td>
</tr>
<tr>
<td>FFPC_4_DA_BUS</td>
<td>65 5 1.7638 2.1811 2</td>
</tr>
<tr>
<td>MULTI_DA</td>
<td>81 7 2.3307 1.5906 1</td>
</tr>
<tr>
<td>FFPC_4_DA</td>
<td>63 2 2.1339 1.6299 1</td>
</tr>
<tr>
<td>FFPC_8_DA_BUS</td>
<td>104 10 2.1339 2.1811 2</td>
</tr>
<tr>
<td>FFPC_8_DA</td>
<td>146 15 2.5039 2.1811 1</td>
</tr>
<tr>
<td>10x16_DA</td>
<td>160 17 2.8740 1.6299 2</td>
</tr>
<tr>
<td>15x15_DA</td>
<td>225 25 3.4409 1.9606 3</td>
</tr>
<tr>
<td>10x30_DA</td>
<td>300 34 3.6142 2.1811 2</td>
</tr>
</tbody>
</table>

Wiring costs for the 21 combinations, sorted in increasing order, showing the adjusted PCB dimensions (after adding room for shift registers (SR)), number of layers and resultant breakdown of costs (PCB and shift registers).

### Metric Selection
The predominant factors that impact PCB costs are the wire-trace width/spacing ($width_t/width_s$), smallest via size ($width_v$), PCB dimensions ($width_{PCB}$, height_{PCB}) and number of layers [2]. Table II shows that the number of layers depends on the orthogonal capacity, which depends on the trace and via metrics, as per Equation (4).

Table III presents parameter combinations that yield a range of orthogonal capacities for 1 mm, 2 mm and 2.54 mm electrodes. Advanced Circuits’ PCB cost estimator provides the following wire trace sizes (all in inches): 0.0025, 0.003, 0.004, 0.005, 0.006, 0.007, 0.008, 0.010 and 0.012. To achieve each orthogonal capacity, we chose the lowest trace size and highest minimum via size such that $width_t \geq 2 \times width_s$ and $width_v \geq width_t + 0.01$; these requirements were relaxed for the smaller 1 mm electrodes (such that $width_{PCB} \geq width_t + 0.003$) because there was not enough space to utilize such conservative size estimates.

For each electrode pitch, we select one set of parameters and report the orthogonal capacity. For 1 mm electrodes, estimations were not available for orthogonal capacities of 4 and 5, and we could not find parameters that could achieve an orthogonal capacity of 6; we conservatively opted for an orthogonal capacity of 2: even as the number of PCB layers increases to 4, the cost is less than a single-layer PCB with orthogonal capacity of 3. Fig. 23 shows a two-layer solution for FFPC_4_MODULE with orthogonal capacity of 2.

For 2 mm and 2.54 mm electrode pitches, we select the metric set corresponding to orthogonal capacities of 4 and 6, respectively. These are the highest capacities before the price increases significantly for each electrode size and reductions in layer count do not typically occur at higher orthogonal capacities, as shown in Table II.

Table III reveals that, in general, as the feature sizes decrease, particularly the wire trace size, the fabrication costs increase, and that 1- and 2-layer solutions are identical for all cases; this is because PCBs can be printed on two sides. Table III reflects this observation, as prices tend to jump more significantly as each odd numbered layer is added, meaning that a new, physical dual-sided PCB layer must be added.

### D. PCB Cost Results
Table IV presents cost results for each DMFB architecture in Table II assuming 1 mm electrode sizes and an orthogonal capacity of 2, as discussed in the preceding subsection. Table IV reports the number of pins and the subsequent number of required shift registers (SR), along with the PCB dimensions, which include extra space allocated for shift registers. The PCB dimensions are fed directly into the online cost estimator. The reported cost of the PCB is estimated under the...
assumption of a 4-week delivery time (slowest) at a quantity of 2500 [2]; the shift registers cost $0.139 apiece at a quantity of 2500 [6]. As described in Equation (2), the total cost is that of the PCB plus shift registers.

In Table IV the DMFB chips are sorted in increasing order of cost, and the results show that FPPC_4_MODULE is the cheapest design by at least $0.18 per board, compared to assay-specific chips ZHAO_XXX and LUO_XXX. The FPPC_4_DA_BUS design, which can transport multiple droplets concurrently because the 3-phase buses are replaced by direct-addressing buses, is $0.56 more expensive than its pin-optimized counterpart. Given that droplet transport times are orders of magnitudes faster than operation times [34][39] and that the FPPC-DMFB with serial routing has proven competitive to pin-constrained assay-specific chips in terms of performance [12], we believe that FPPC_4_MODULE is the best overall solution when considering price and performance.

Table IV also shows that the PCB cost for many directly addressable DMFBs is less expensive than pin-constrained counterparts. For example, even though PCR_DA is 0.4 in longer than LUO_PCR, the PCB is $0.47 cheaper because it requires fewer layers; however, the directly addressable version requires 5 shift registers, increasing the cost of the design to be $0.23 more expensive than LUO_PCR.

This overall trend of shift-register costs is shown in the bottom half of Table IV: starting with PROTEIN_DA and looking downward, the number of pins, shift registers and total cost are non-decreasing. Thus, it is important to minimize the pin-count; however, it must be balanced with a reduction in the number of PCB layers, as seen with our FPPC-DMFB, to achieve a comparably low-cost wire-routing solution.

Fig. 24 presents the final cost estimates for each of the 21 DMFBs with 1 mm, 2 mm and 2.54 mm electrodes, using the parameters reported in Table III, and the shift register costs described previously. All estimates assumed for a 4-week delivery time and shipment quantity of 1000 because price estimates of 2500 could not be obtained online for all benchmarks. The benchmarks are sorted, from left to right, in order of increasing average cost. Although there is some variation when comparing the cost between different electrode sizes (e.g., from MULTI_DA to LUO_INVITRO, the 1 mm and 2 mm costs decrease, while the 2.54 mm cost increases), the overall trend of increasing price follows the average for each electrode pitch. This indicates that electrode pitch minimally impacts PCB cost since the manufacturing parameters can be adjusted to compensate the orthogonal capacity to reduce the number of layers.

For several of the benchmarks, the 1 mm boards are more expensive than their 2 mm counterparts. Recall that shift registers are stacked vertically and that additional width is added in the X-dimension to accommodate new columns, as necessary. Since the 2 mm instances provide a greater PCB height (height_{PCB}) than the 1 mm instances, the 2 mm boards sometimes require less additional space (width_{PCB,SR}) to accommodate the extra shift registers, which indirectly offsets the initial area cost of using larger electrodes. This occurs, for example, for FPPC_4_DA and FPPC_8_DA. The extra cost for 15x15_DA is due to an additional layer (3 vs. 2 layers) for the smaller 1 mm case, due to its lower orthogonal capacity.

E. Routing Performance

The top portion of Table V reports the time spent performing operations and routing on 9 common benchmark assays [12][14][16][34] for sequential (pin-optimized) and parallel (route-optimized) FPPC-DMFBs, with and without wash droplets; identical schedules were used for both chips. The width of the chip is increased to 11 electrodes, to make room for the two wash I/O reservoirs. All but one benchmark was performed with the standard 16-electrode height, as shown in Fig. 7, allocating 4 mix modules, 5 SSD modules and 1 routing buffer; the ProteinSplit3 benchmark requires a larger 11x18 array with an extra SSD module. The results show that the parallel routing version (without wash droplets) yields a modest 1-10% savings (up to 4.29s on ProteinSplit3); however, when wash droplets are introduced, parallel routing on the route-optimized FPPC-DMFB reduces the overall completion time by 6-28% (up to nearly 18s on ProteinSplit3).

Using the preferred metrics for 2 mm electrodes in Table III, the price for an 11x16 pin-optimized (sequential) and route-optimized (parallel) FPPC-DMFB are $1.44 and $2.00, respectively. Thus, as expected, the modest gains in performance for the route-optimized FPPC-DMFB come at the expense of cost. Ultimately, the end user should decide which tradeoff to take when considering their desired application and...
whether cost or performance is more important.

The bottom portion of Table V gives results for a state-of-the-art direct addressing synthesis flow [14]. We use a similarly sized array (11x16 vs. 15x11), although the direct addressing device is wider since it is a better fit for its virtual topology. The virtual topology configuration of the direct addressing model dictates that a 15x11 DMFB can allocate four general-purpose modules, which can process mixes, splits or two simultaneous storage operations [14]. The results show that the direct addressing design is able to obtain better routing results because of its flexibility and extra electrodes; however, although the route saving percentages are high, the actual route savings do not grow larger than 2.5s. In contrast, as seen from the schedule lengths, the FPPC-DMFB is able to produce significantly better schedules (savings almost 40s with ProteinSplit3). Thus, the overall savings show that the FPPC-DMFB produces superior performance results as the assay size increases. Finally, using the preferred metrics for 2mm electrodes in Table III, the price for a 15x11 direct addressing DMFB is $4.22, which is $2.22 to $2.78 more expensive than the 11x16 FPPC-DMFBs that perform the same assays.

VIII. CONCLUSION

This paper has extended the initial development of FPPC-DMFBs [12] with an enhanced design to facilitate more efficient wire routing, and has presented the first cost estimates, in terms of US dollars, for PCB fabrication for DMFBs. A complete synthesis flow, which addresses architectural issues that are specific to the FPPC-DMFB, has been presented, along with a detailed description of its general-purpose, as opposed to assay-specific, capabilities.

Our prior work has shown that the general-purpose FPPC-DMFB is competitive with direct-addressing and prior pin-constrained assay-specific DMFBs in terms of performance [12]; this work goes one step further by showing that the FPPC-DMFB is less expensive than previous pin-constrained designs, when optimized for cost and PCB design. Thus, the flexibility provided by the FPPC-DMFB is unmatched by prior pin-constrained DMFBs, which were optimized for specific assays, and offers a significant advancement in terms of programmability at a lower overall per-unit cost.

IX. ACKNOWLEDGMENT

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[2] www.4pcb.com


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