

4BIT REAL TIME CLOCK MODULE with I/O CONNECTIONS

RTC-58321/58323

Overview

The RTC-58321/58323 is a CMOS real time clock modules with perpetual calendar function developed for microcomputer applications.

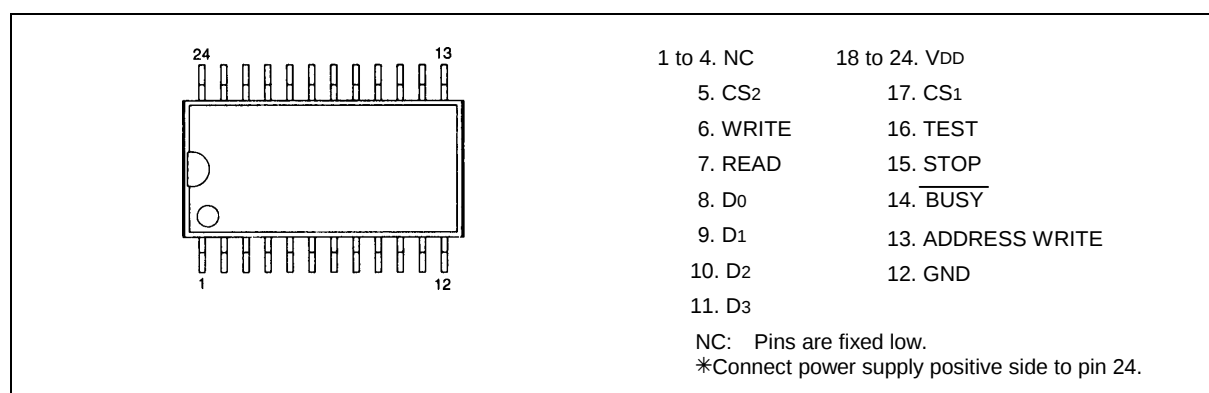
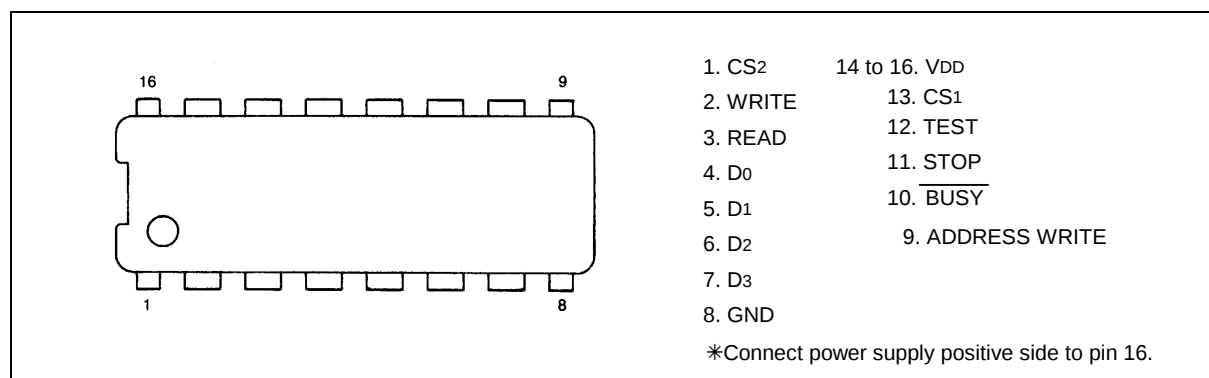
It has a built-in 32.768 kHz quartz resonator, and provides clock and calendar registers for year, month, day, day-of-week, hours, minutes and seconds, with 12-hour/24-hour selection, plus automatic leap-year correction with software selection for local calendars, and an additional periodic reference signal output.

Being a CMOS device, it has a very low power consumption for battery back-up purposes.

Features

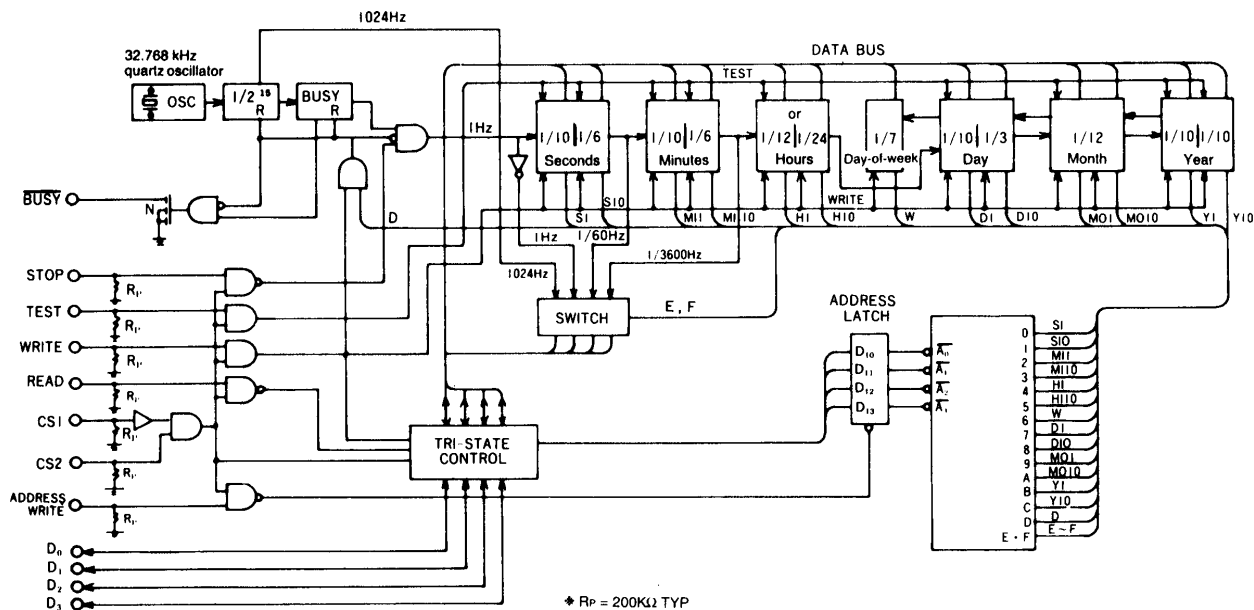
- Adjustment-free built-in quartz resonator keeps component count low.
- Built-in clock and calendar registers for year, month, day, day-of-week, hours, minutes and seconds.
- 12-hour/24-hour selection.
- Automatic leap-year correction, with software selection for local calendars.
- Counter start, stop and reset functions.
- Periodic reference signal output selectable: 1024 Hz, or 1 second, 1 minute or 1 hour intervals.
- Data bus is 4-bit bi-directional, with memory-type reads and writes.
- CMOS device, for very low power consumption, and long battery back-up period.
- Compatible at pin and function levels with the MSM58321 RS.

Pin connections



RTC-58321/58323

Block diagram



Pin functions

Pin numbers		Pin symbol	Input/output	Function
RTC-58321	RTC-58323			
1	5	CS2	Input	Chip select. When high, device can be accessed.
2	6	WRITE	Input	Set high to write.
3	7	READ	Input	Set high to read.
4 to 7	8 to 11	D0 to D3	Both	Address/data bus.
8	12	GND		Negative power supply.
9	13	ADDRESS WRITE	Input	Address latch. Set high to latch address from D0 to D3.
10	14	BUSY	Output	1 Hz output pin.
11	15	STOP	Input	1 Hz on/off control pin. When high, the 1 Hz signal is disabled, and the counter stopped.
12	16	TEST	Input	Increment pin for the counter. Normally this pin should be fixed low.
13	17	CS1	Input	Connect to power down detection circuit. (Fix high if there is no power down detection circuit.) When CS1 is low, chip cannot be accessed, regardless of state of CS2.
*	1 to 4	NC		Fix low.
14 to 16	18 to 24	VDD		Positive power supply (normally +5 V).

* A bypass capacitor (minimum 0.01 μF) must be connected between VDD and GND, as close as possible.

■ Characteristics

1. Absolute maximum ratings

Item	Symbol	Conditions (Pins)	Rated Value		Unit
Power supply voltage	VDD	Ta = 25°C, VDD-GND	-0.3 to +7.0		V
Input voltages	Vi	Ta = 25°C input pins	-0.3 to VDD +0.3		V
Output voltages	Vo	D0 to D3	-0.3 to VDD +0.3		V
Storage temperature	TSTG	Temperature stored as separate item.	RTC-58321	-55 to +85	°C
			RTC-58323	-55 to +125	°C
Soldering temperature	TSOL	RTC-58321	Maximum 260 °C for up to 10 seconds (pins); package maximum 150 °C.		
		RTC-58323	Maximum 260 °C for up to 10 seconds (twice maximum), or maximum 230 °C for up to three minutes.		

2. Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Notes
Power supply		VDD	4.5	5.0	5.5	V	VDD-GND
Data hold voltage *1		V _{DH}	2.2	-	5.5		
Operating temperature	RTC-58321	TOP	-10	-	70	°C	
	RTC-58323		-30	-	85		

*1 Data hold voltage: This is the range of power supply voltage for which the internal operation of the clock is guaranteed. I/O operations are not guaranteed.

3. Frequency characteristics

Item		Symbol	Conditions	Max.	Unit
Frequency tolerance	RTC-58321 A	$\Delta f/f_0$	Ta = 25°C VDD = 5.0V	± 10	ppm
	RTC-58321 B			± 50	
	RTC-58323			5 ± 20	
Aging		fa	Ta = 25°C; VDD = 5.0V; first year	± 5	ppm/y
Temperature characteristics *2		tOP	VDD = 5.0V; Ta = -10 to 70°C	+ 10/-120	ppm
Voltage characteristics		fV	VDD = 2.2 to 5.5V Ta fixed, 5V reference	± 2	ppm

*2 Deviation from the frequency at 25 °C.

Notes 1. Frequency tolerance based on VDD = 5.0 V.
2. Frequency tolerance is value guaranteed on factory shipment.

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4. DC characteristics

RTC-58321 (V_{DD} = 5V ± 0.5V, Ta = -10 to 70°C)
RTC-58323 (V_{DD} = 5V ± 0.5V, Ta = -30 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage	V _{IH1} *1		3.6			V
	V _{IH2} *2		V _{DD} - 0.5			V
Low input voltage	V _{IL}				0.8	V
Low output voltage	V _{OL}	I _{OL} = 1.6mA			0.4	V
Low output current	I _{OL}	V _{OL} = 0.4V	1.6			mA
High input current	I _{IH} *3	V _{IH} = 5V	10	30	80	μA
Low input current	I _{IL} *3	V _{IL} = 0V			-1	μA
Input leakage current	I _{LIH}	V _{IH} = 5V			1	μA
Input off-state leakage current	I _{LIL}	V _{IL} = 0V			-1	
Input capacity	C _i	f = 1MHz		5		pF
Current consumption	I _{OP}	V _{DD} = 5V	*4	100	500	μA
			*5	20	40	
		V _{DD} = 3V	*4	15	30	
			*5	7	20	
Oscillation start time *6	t _{osc}	V _{DD} = 5V Ta = 25°C		1.5	3.0	sec.

*1 Pins CS₂, WRITE, READ, ADDRESS WRITE, STOP, TEST and D₀ to D₃

*2 CS₁

*3 Pins CS₁, CS₂, WRITE, READ, ADDRESS WRITE, STOP and TEST

*4 CS₁ and CS₂ high, $\overline{\text{BUSY}}$ Open-circuit

*5 CS₁, CS₂ and $\overline{\text{BUSY}}$ Open-circuit

*6 Confirmed by $\overline{\text{BUSY}}$

5. AC characteristics

RTC-58321 (V_{DD} = 5V ± 0.5V, Ta = -10 to 70°C)
RTC-58323 (V_{DD} = 5V ± 0.5V, Ta = -30 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Chip select set-up time	t _{CS}	-	0	-	-	μS
Address set-up time	t _{AS}	-	0	-	-	μS
Address write pulse width	t _{AW}	-	0.5	-	-	μS
Address hold time	t _{AH}	-	0.1	-	-	μS
Data set-up time	t _{DS}	-	0	-	-	μS
Write pulse width	t _{WW}	-	2	-	-	μS
Data hold time	t _{DH}	-	0	-	-	μS
Read inhibit time	t _{RI}	-	0	-	-	μS
Read access time	t _{RA}	-	-	-	*	μS
Read delay time	t _{DD}	-	-	-	1	μS
Chip select hold time	t _{CH}	-	0	-	-	μS

*
$$t_{RA} = 1\mu S + C \times R \times \ln \frac{V_{DD}}{V_{DD} - V_{Hmin}}$$

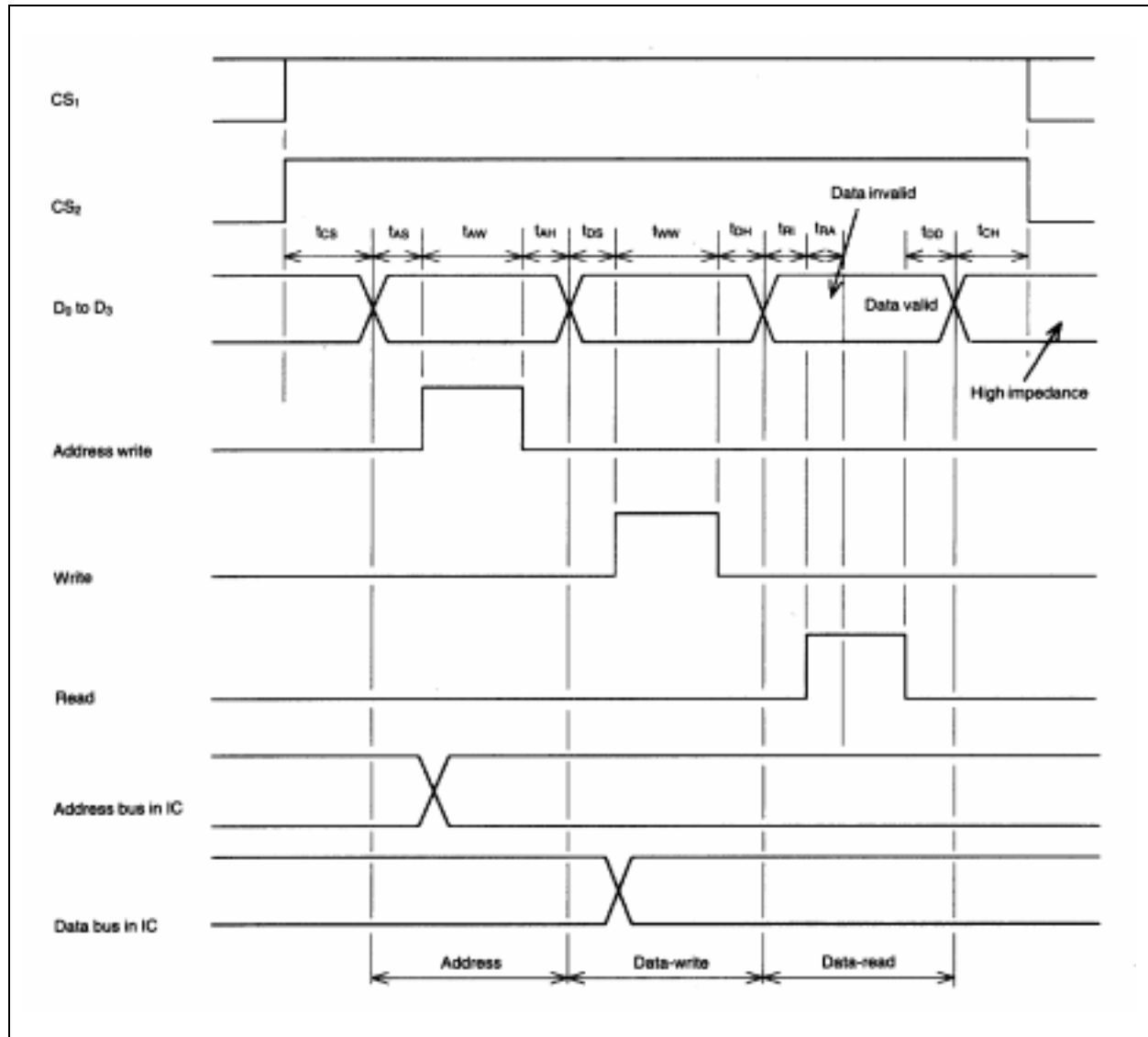
C : capacitance of data line

R : pull-up resistance

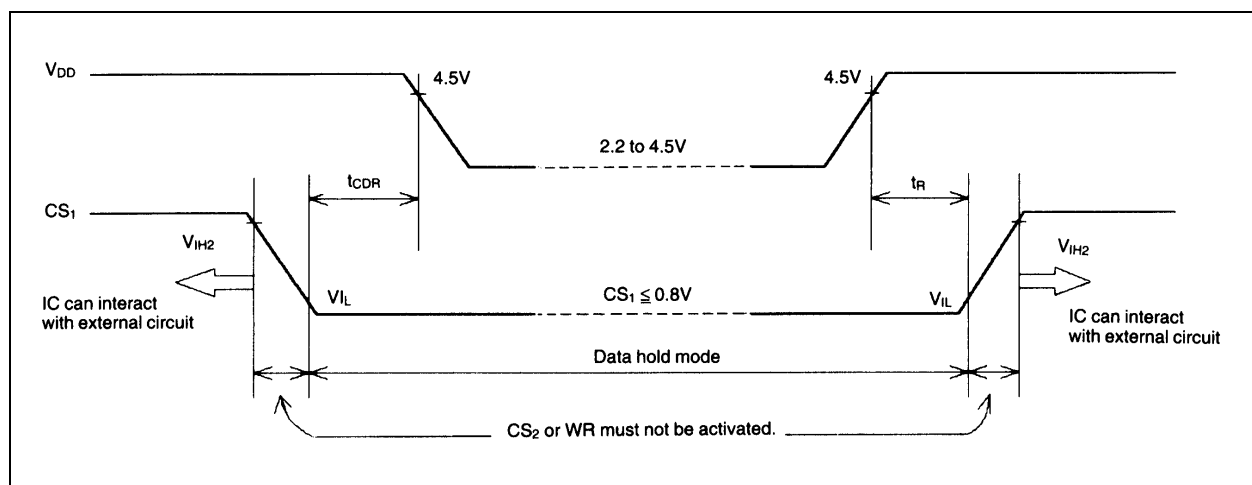
V_{Hmin} : high voltage level of IC connected to data line

ln : natural logarithm

6. Timing chart



7. Data hold timing



Registers

1. Register table

Address (hexadecimal)	D3 (A3)	D2 (A2)	D1 (A1)	D0 (A0)	Register name	DATA				Count value	Notes	
	D3	D2	D1	D0								
0	0	0	0	0	S1	s8	s4	s2	s1	0 to 9	Seconds units register	
1	0	0	0	1	S0	*	s40	s20	s10	0 to 5	Seconds tens register	
2	0	0	1	0	M1	mi8	mi4	mi2	mi1	0 to 9	Minutes units register	
3	0	0	1	1	M10	*	mi40	mi20	mi10	0 to 5	Minutes tens register	
4	0	1	0	0	H1	h8	h4	h2	h1	0 to 9	Hours units register	
5	0	1	0	1	H10	24/12	pm/am	h20	h10	0 to 1 or 0 to 2	Hours tens register	
6	0	1	1	0	W	*	w4	w2	w1	0 to 6	Day-of-week register	
7	0	1	1	1	D1	d8	d4	d2	d1	0 to 9	Day units register	
8	1	0	0	0	D10	Leap year select		d20	d10	0 to 3	Day tens register	
9	1	0	0	1	MO1	m08	m04	m02	m01	0 to 9	Month units register	
A	1	0	1	0	MO10	*	*	*	m010	0 to 1	Month tens register	
B	1	0	1	1	Y1	y8	y4	y2	y1	0 to 9	Year units register	
C	1	1	0	0	Y10	y80	y40	y20	y10	0 to 9	Year tens register	
D	1	1	0	1		*	*	*	*		Reset register	
E	1	1	1	0			1hour	1minute	1second	1024Hz		Reference signal registers
F	1	1	1	1								

2. Notes

- (1) The device uses positive logic, and a logic high voltage corresponds to a 1 in a register bit.
- (2) Do not set the clock to impossible dates (17:34 pm on February 30th, for example). The results are unpredictable.
- (3) When the device is powered on, the initial settings of all bits are undefined.

Register functions

1. Date and time registers

- (1) The register values are in BCD, and used positive logic.

E.g. (S8, S4, S2, S1) = (1, 0, 0, 1) = 9 seconds

- (2) Day-of-week register

The value is coded as 0 to 6, with Sunday = 0.

Code	0	1	2	3	4	5	6
Day	Sun.	Mon.	Tue.	Wed.	Thud.	Fri.	Sat.

- (3) pm/am, h20 and h10 registers

The range of these values depends on whether the 12-hour or 24-hour clock is being used.

The pm/am bit is used only when the 12-hour clock is selected.

Set D3 to 1 for the 24-hour, and to 0 for the 12-hour clock.

Set D2 to 1 for pm and to 0 for am. Writing a 1 to bit D3 automatically resets bit D2 to 0.

Selection	Value range
12-hour clock	12:00 to 11:59 am and pm *
24-hour clock	00:00 to 23:59

* Note: 12:00 am represents 12:00 midnight, and 12:00 pm represents 12:00 noon.

- (4) Y1 and Y10 Leap year selection

Bits D3 and D2 of the day tens register select the year value module 4 to be used for leap years.

Calendar	D3	D2	Value module 4 for leap year
Standard calendar	0	0	0
	0	1	3
	1	0	2
	1	1	1

- (5) Do not set the clock to impossible dates (17:34 pm on February 30th, for example). The results are unpredictable.

2. Reset register (Control register D)

Select this register to reset the last five stages of the $1/2^{15}$ divider, and the busy circuit.

Latch the hexadecimal value D using the ADDRESS LATCH pin, and set WRITE high to carry out the reset.

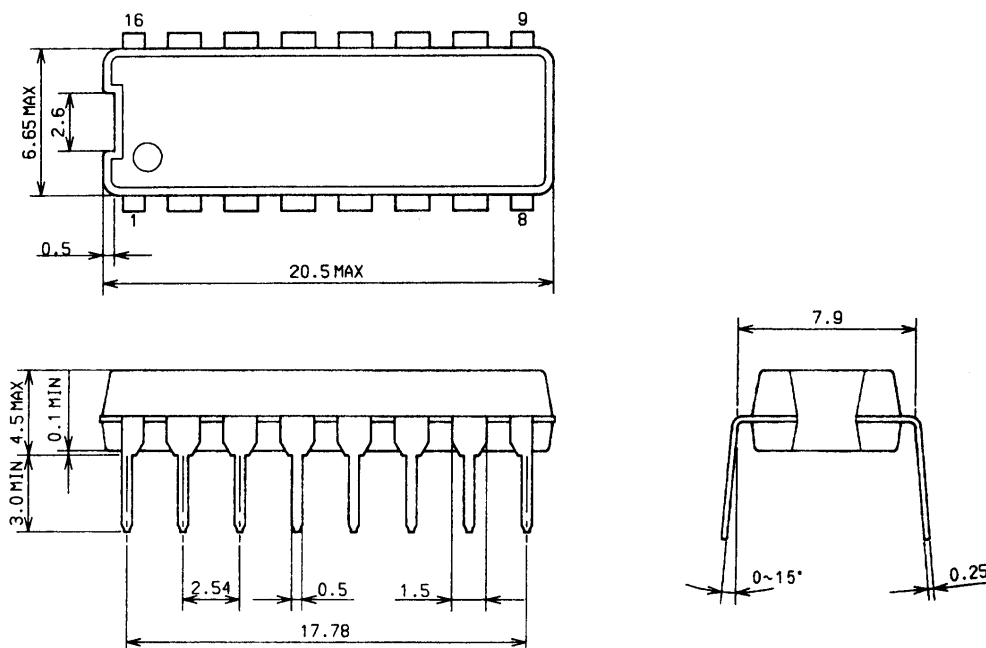
3. Reference signal (Control registers E and F)

Latch the hexadecimal value E or F using the ADDRESS LATCH pin, and set WRITE high to obtain the reference signal values on D0 to D3.

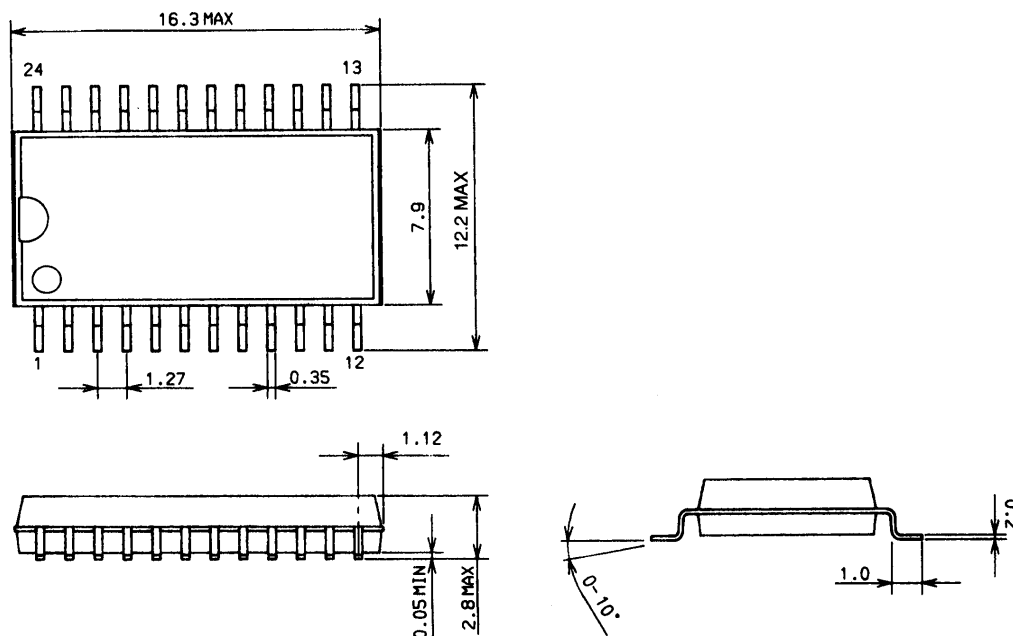
■ Package dimensions

(1) RTC-58321

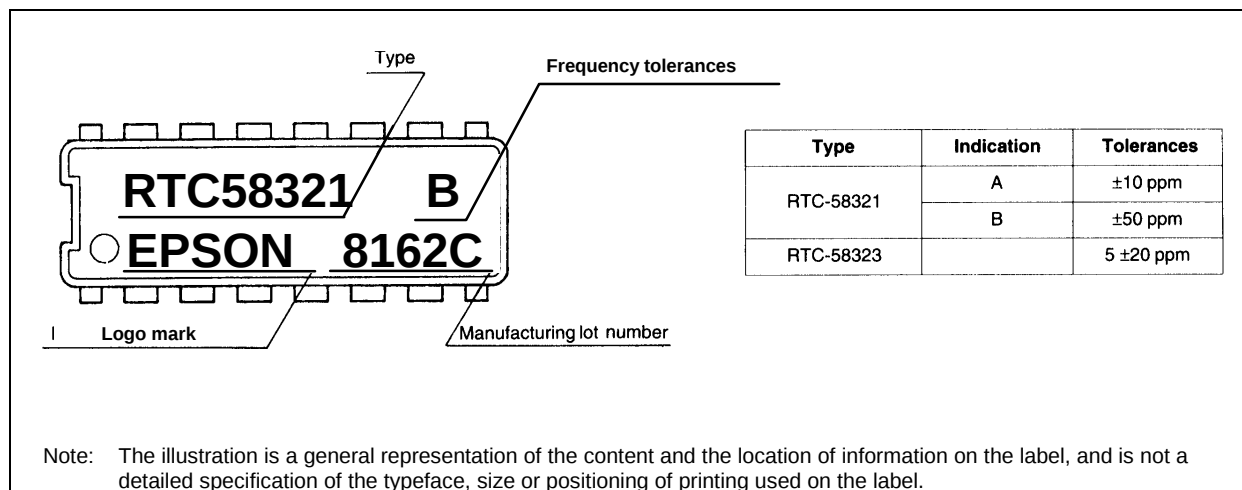
(Unit:mm)



(2) RTC-58323

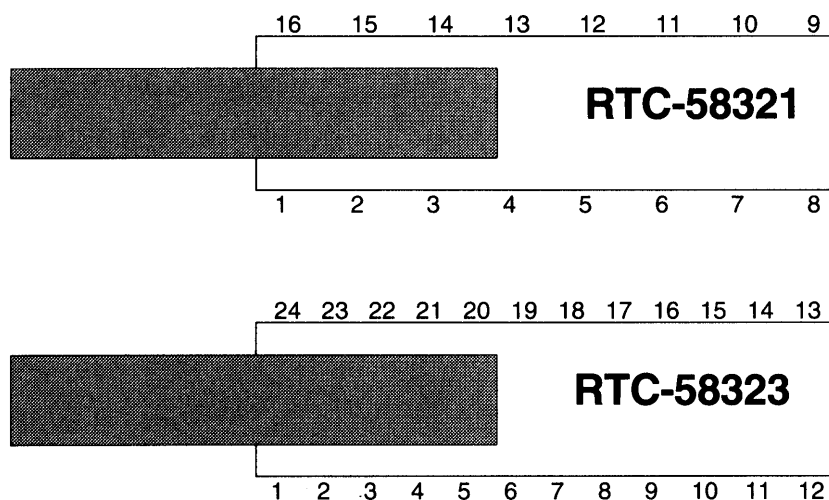


■ Marking layout



■ Application notes

- (1) In order to realize low-power operation, the device has a high impedance; the shaded portion in the figure below is highly susceptible to inductance effects, and should be kept clear of signal lines.



- (2) Power supply filter capacitor
To ensure stable operation against transients and noise, connect a bypass capacitor of at least 0.01 μ F (ceramic) across the power supply, close to the device.
- (3) This device passes a drop test (from 75 cm onto a hard board), but it is possible for the crystal resonator to be damaged by the shocks produced by some mounting equipment. It is important to confirm that the mounting conditions for the equipment being used do not adversely affect performance. Re-check if any of the mounting conditions change.
- (4) There is a possibility of damage to the crystal resonator during ultrasonic cleaning. Because of the wide variation of conditions in ultrasonic cleaning equipment, the performance of this device is not guaranteed if it is subject to ultrasonic cleaning.
- (5) This is a CMOS device, and the standard precautions against static electricity should be taken.

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