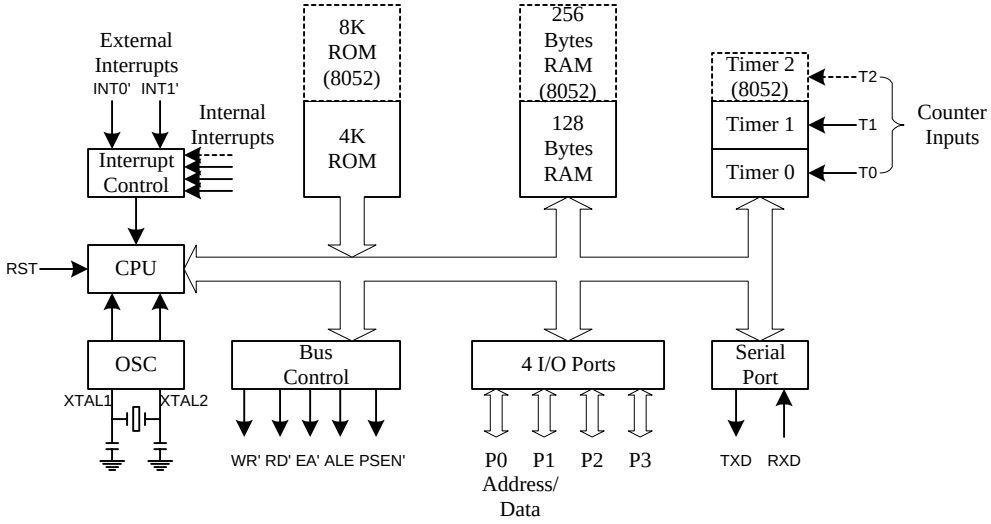
8051 Hardware Overview

- 3 basic versions of the MCS-51:

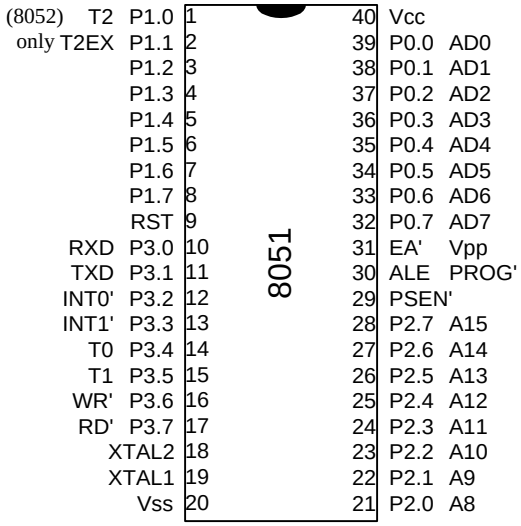
	ROM	RAM	I/O lines	Counter/Timers	Interrupt
8051	4K bytes	128 bytes	32	2 – 16 bit	5 (2 ext)
8031	none				“
8751	same as 8051 but with EPROM				“
8052	8K bytes	256 bytes		3 – 16 bit	6 (2 ext)
8032					“
8752					“

- a duplex serial port
- bit-level Boolean processor

8051 Block diagram

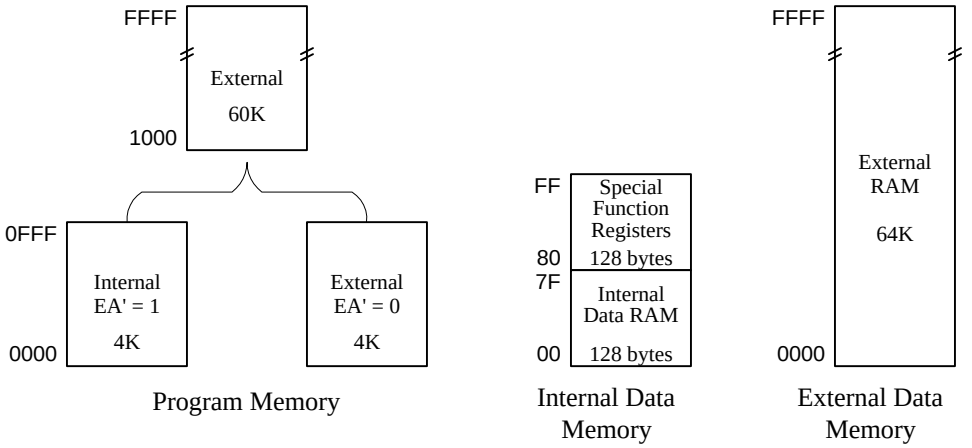


8051 Pinout



WR' – Write strobe to write external data memory.
RD' – Read strobe to read external data memory.
EA' – External address strobe for the 4K bytes of program memory.
EA' = 0 for external 4K ROM.
EA' = 1 for internal ROM.
ALE – Address latch enable for latching the address signals on P0.
ALE = 1 for latching address signals on P0.
ALE = 0 for latching data signals on P0.
PSEN' – Program store enable for reading external program memory.

Memory map



Number of address lines	Number of bytes addressed in decimal (hex)
1	2
2	4
3	8
4	16 (10)
5	32 (20)
6	64 (40)
7	128 (80)
8	256 (100)

Number of address lines	Number of bytes addressed in decimal (hex)
9	512 (200)
10	1024=1K (400)
11	2048=2K (800)
12	4096=4K (1000)
13	8192=8K (2000)
14	16384=16K (4000)
15	32768=32K (8000)
16	65536=64K (10000)

Interrupt vector addresses in program memory

Timer 2 interrupt →		002B
Serial port interrupt →		0023
Timer 1 interrupt →		001B
External interrupt 1 →		0013
Timer 0 interrupt →		000B
External interrupt 0 →		0003
Reset →		0000

The first 256 bytes of internal data memory

F8									Special function registers (SFR) (128 bytes)
F0	B								
E8									
E0	ACC								
D8									
D0	PSW								
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2			
C0									
B8	IP								
B0	P3								
A8	IE								
A0	P2								
98	SCON	SBUF							
90	P1								
88	TCON	TMOD	TL0	TL1	TH0	TH1			
80	P0	SP	DPL	DPH				PCON	
78									Scratch pad area (80 bytes)
70									
68									
60									
58									
50									
48									
40									
38									
30									
28	Can be addressed as 16 bytes or 128 individual bits. Byte addresses are 20H to 2F. Bit addresses are 00H to 7F.								
20									
18	Reg 0	Reg 1	Reg 2	Reg 3	Reg 4	Reg 5	Reg 6	Reg 7	Bank 3
10	Reg 0	Reg 1	Reg 2	Reg 3	Reg 4	Reg 5	Reg 6	Reg 7	Bank 2
8	Reg 0	Reg 1	Reg 2	Reg 3	Reg 4	Reg 5	Reg 6	Reg 7	Bank 1
0	Reg 0	Reg 1	Reg 2	Reg 3	Reg 4	Reg 5	Reg 6	Reg 7	Bank 0

ACC – Accumulator
B – B register for multiply and divide.
PSW – program status word
- PSW.7 – Carry flag (CY)
- PSW.6 – Auxiliary carry flag (AC)
- PSW.5 – User define
- PSW.4 & 3 – Register bank select (RS1, RS0): 00=Bank 0; 01=Bank 1; 10=Bank 2; 11=Bank 3
- PSW.2 – Overflow flag (OV)
- PSW.1 – User define
- PSW.0 – Parity flag (P)

SP – Stack pointer. Initialized to 07H. SP is incremented before data is pushed on the stack.
DPTR – Data pointer (DPH, DPL). To store a 16-bit address for certain instructions.
P0, P1, P2, P3 – Port latches matching the 4 I/O ports.
SBUF – Serial data buffer. Read and write registers for the serial port.
SCON – Serial port control.
TMOD – Timer mode.
TCON – Timer control.
T2CON – 8052 timer 2 control.

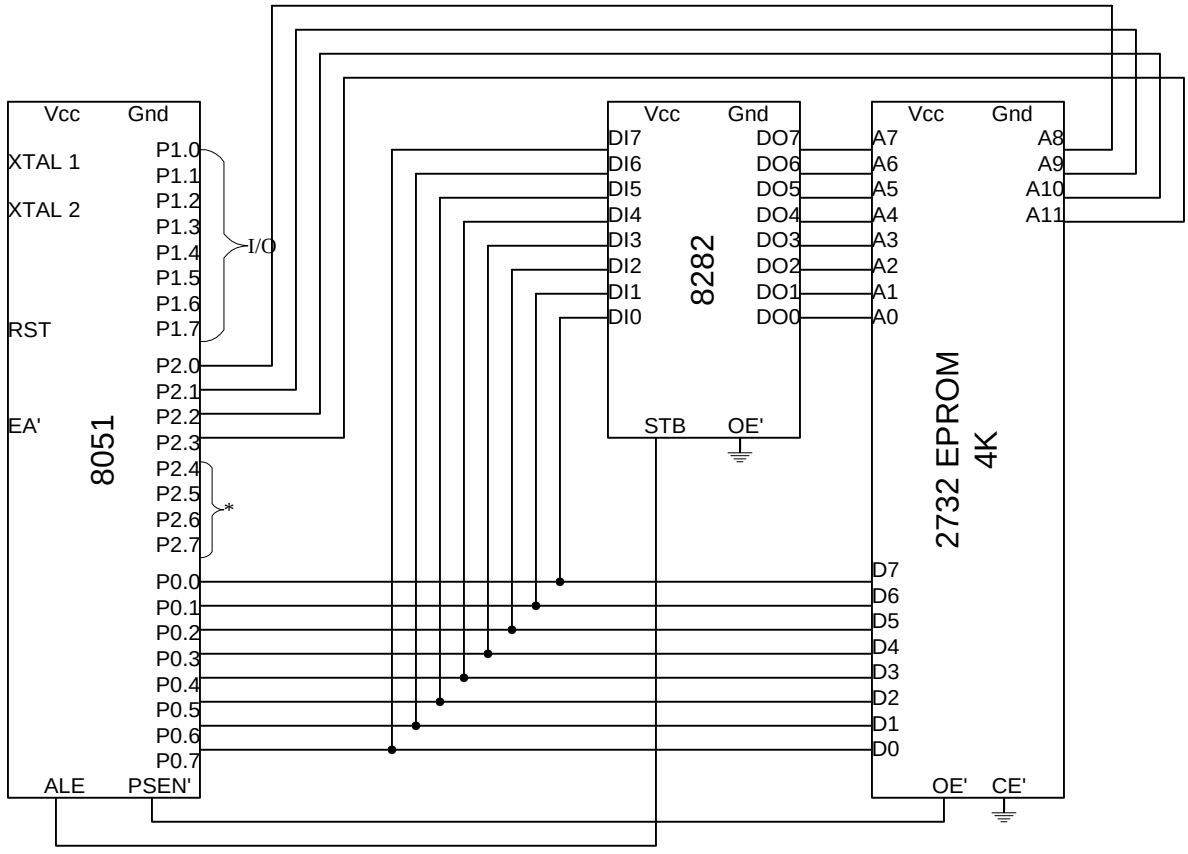
PCON – Power control. Use in the 80C51 only.
IE – Interrupt enable. 1=enable; 0=disable.
- IE.7 – all interrupts (EA).
- IE.6 – not used.
- IE.5 – timer 2 (ET2). (8052 only).
- IE.4 – serial port (ES).
- IE.3 – timer 1 (ET1).
- IE.2 – external interrupt 1(EX1).
- IE.1 – timer 0 (ET0).
- IE.0 – external interrupt 0 (EX0).

source IE0.	interrupt address at 002B.
source TF0.	interrupt address at 0023.
source IE1.	interrupt address at 001B.
source TF1.	interrupt address at 0013.
source R1 & T1.	interrupt address at 000B.
source TF2 & EXF2.	interrupt address at 0003.

IP – Interrupt priority. 1=high priority; 0=low priority.
- IP.7 – not used.
- IP.6 – not used.
- IP.5 – timer 2 (PT2). (8052 only).
- IP.4 – serial port (PS).
- IP.3 – timer 1 (PT1).
- IP.2 – external interrupt 1 (PX1).
- IP.1 – timer 0 (PT0).
- IP.0 – external interrupt 0 (PX0).

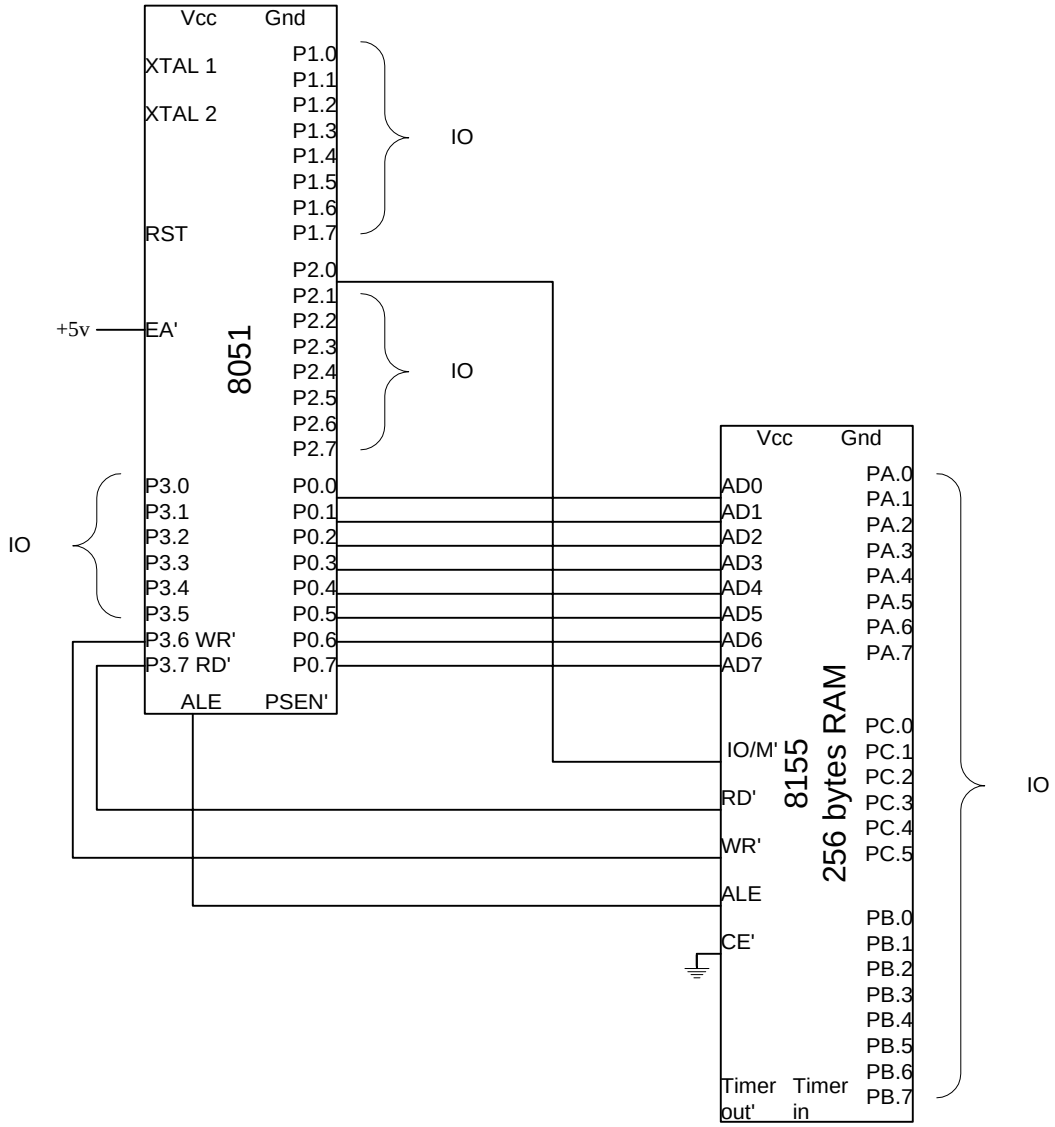
RCAP2L – 8052 only.

External program memory using a 2732 4K EPROM



* These pins are not available as I/O when any part of Port 2 is being used as an address bus.

External RAM and I/O



Address Lines	Decimal	Hex
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2	4	4
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7	128	80
8	256	100

Address Lines	Decimal	Hex
9	512	200
10	(1K) 1024	400
11	(2K) 2048	800
12	(4K) 4096	1000
13	(8K) 8192	2000
14	(16K) 16384	4000
15	(32K) 32768	8000
16	(64K) 65536	10000

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0