UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering
CS/EE120B – Introduction to Embedded Systems
Midterm 1
August 6, 2003

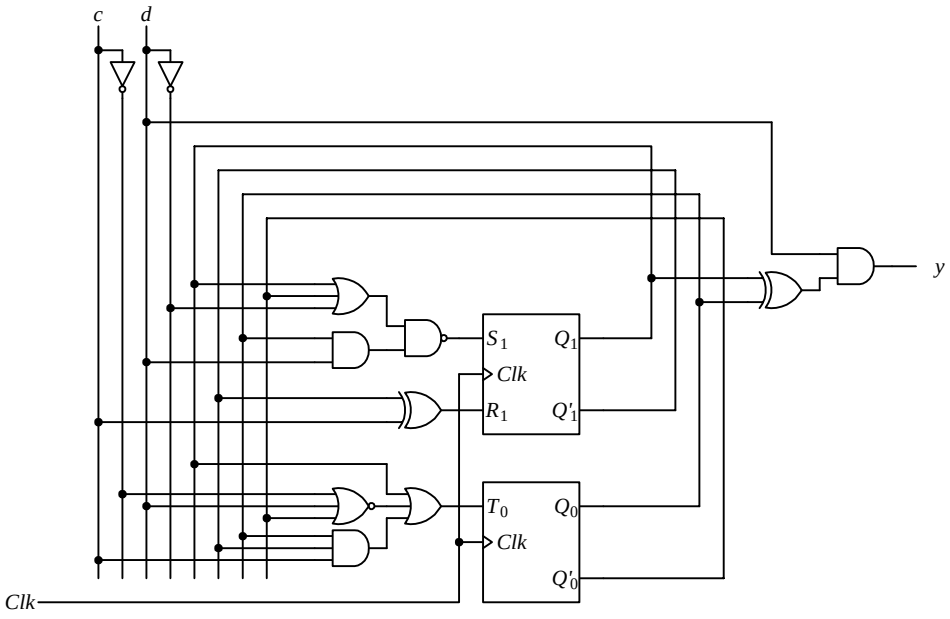
18

Name: Solution Key **Student ID#:** _____

Please print legibly

(Numbers in parenthesis denote total possible points for question.)

1. Analyze the following FSM and draw the state diagram for it. (6)



Answer

Excitation equations:

$S_1 = [(Q_1 + Q_0' + d')\,(Q_0\, d)]'$
$= [dQ_1Q_0 + \cancel{dQ_0Q_0'} + \cancel{dd'Q_0}]'$
$= (dQ_1Q_0)'$
$= d' + Q_1' + Q_0'$

$R_1 = Q_1' \oplus c$

$T_0 = Q_1 + (c' + d + Q_0')' + (Q_0Q_1'c)$
$= Q_1 + (cd'Q_0) + (cQ_1'Q_0)$

Characteristic equations:

SR ff: $Q_{next} = S + R'Q$
T ff: $Q_{next} = T \oplus Q$

Next-state equations:

$Q_{1next} = S_1 + R_1' Q_1$
$= (d' + Q_1' + Q_0') + (Q_1' \oplus c)' Q_1$
$= (d' + Q_1' + Q_0') + (Q_1 \oplus c) Q_1$
$= (d' + Q_1' + Q_0') + (cQ_1' + c'Q_1) Q_1$
$= (d' + Q_1' + Q_0') + \cancel{cQ_1'Q_1} + c'Q_1\cancel{Q_1}$
$= d' + Q_1' + Q_0' + c'Q_1$

$Q_{0next} = T_0 \oplus Q_0$
$= [Q_1 + cd'Q_0 + cQ_1'Q_0] Q_0' + [Q_1 + (cd'Q_0) + (cQ_1'Q_0)]' Q_0$
$= [Q_1Q_0' + \cancel{cd'Q_0Q_0'} + \cancel{cQ_1'Q_0Q_0'}] + [Q_1' (cd'Q_0)' (cQ_1'Q_0)'] Q_0$
$= [Q_1Q_0'] + [Q_1' (c'+d+Q_0') (c'+Q_1+Q_0')] Q_0$
$= Q_1Q_0' + Q_1' (c'+d+Q_0') (c'+Q_1+Q_0') Q_0$
$= Q_1Q_0' + c'c'Q_1'Q_0 + \cancel{c'Q_1Q_1'Q_0} + \cancel{c'Q_0'Q_1'Q_0} + dc'Q_1'Q_0 + \cancel{dQ_1Q_1'Q_0} + \cancel{dQ_0'Q_1'Q_0} + \cancel{Q_0'c'Q_1'Q_0} + \cancel{Q_0'Q_1Q_1'Q_0} + \cancel{Q_0'Q_0'Q_1'Q_0}$
$= Q_1Q_0' + c'Q_1'Q_0 + c'dQ_1'Q_0$

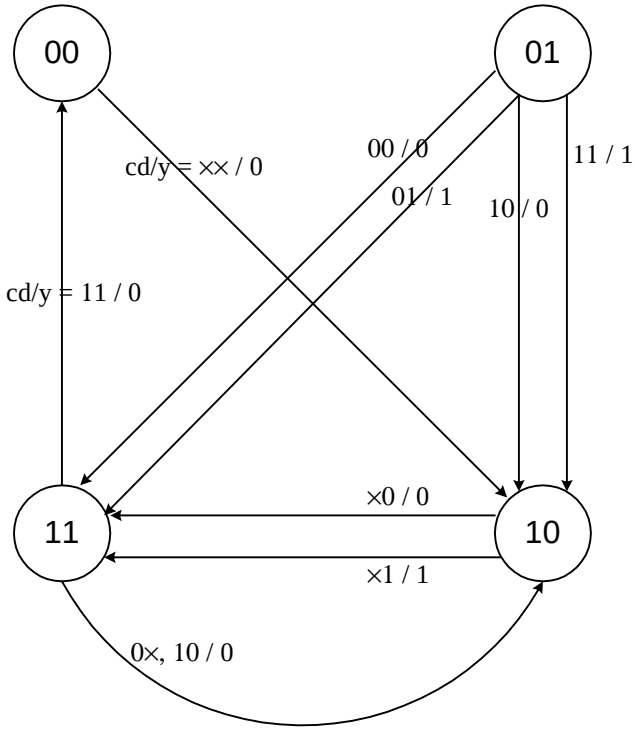
Output equation:

$Y = d (Q_1 \oplus Q_0)$

Next-state and Output table:

Current state Q_1Q_0	Next state / Output $Q_{0next}\ Q_{0next}$ / Y			
	cd =			
	00	01	10	11
00	10/0	10/0	10/0	10/0
01	11/0	11/1	10/0	10/1
10	11/0	11/1	11/0	11/1
11	10/0	10/0	10/0	00/0

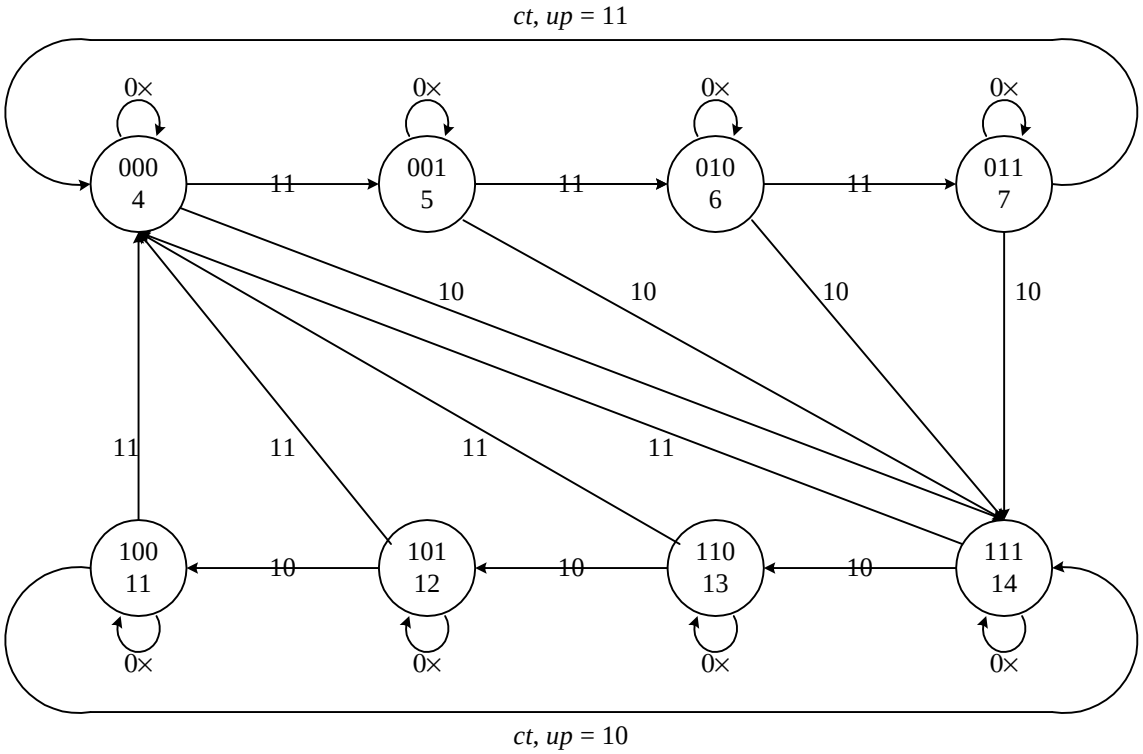
Circuit:



2. Synthesize a FSM for an up/down counter. There are two inputs: up and count. When up is asserted, the counter counts up, otherwise, it counts down. The counter counts when count is asserted, otherwise, the counter stops counting. In the up direction, the counter outputs the numbers 4, 5, 6, and 7 repeatedly in binary. In the down direction, the counter outputs the numbers 14, 13, 12, and 11 repeatedly in binary. When the input up changes, the counter starts from the first number in the counting sequence, i.e. 4 in the up direction and 14 in the down direction. Reduce all combinational circuit equations to standard forms. (6)

Answer

State diagram:



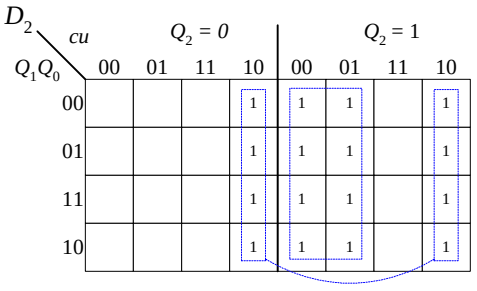
Next-state table:

Current state $Q_2Q_1Q_0$	Next state $Q_{2next}\ Q_{1next}\ Q_{0next}$			
	ct, *up* =			
	00	01	10	11
000	000	000	111	001
001	001	001	111	010
010	010	010	111	011
011	011	011	111	000
100	100	100	111	000
101	101	101	100	000
110	110	110	101	000
111	111	111	110	000

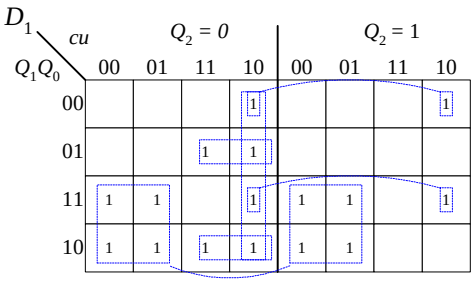
Implementation table:

Current state $Q_2Q_1Q_0$	Implementation $D_2\ D_1\ D_0$			
	ct, *up* =			
	00	01	10	11
000	000	000	111	001
001	001	001	111	010
010	010	010	111	011
011	011	011	111	000
100	100	100	111	000
101	101	101	100	000
110	110	110	101	000
111	111	111	110	000

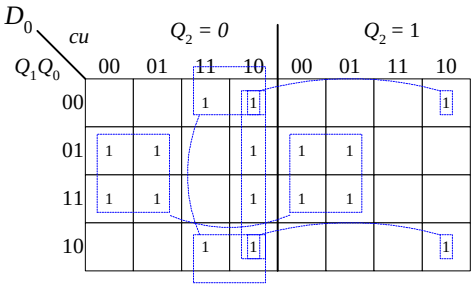
K-maps:



$D_2 = c'Q_2 + cu'$



$D_1 = c'Q_1 + cu'Q_2' + cQ_2'Q_1'Q_0 + cQ_2'Q_1Q_0' + cu'Q_1'Q_0' + cu'Q_1Q_0$



$D_0 = c'Q_0 + cu'Q_2' + cQ_2'Q_0' + cu'Q_1'Q_0' + cu'Q_1Q_0'$

Output Table:

Q_2	Q_1	Q_0	Decimal	Out_3	Out_2	Out_1	Out_0
0	0	0	4	0	1	0	0
0	0	1	5	0	1	0	1
0	1	0	6	0	1	1	0
0	1	1	7	0	1	1	1
1	0	0	11	1	0	1	1
1	0	1	12	1	1	0	0
1	1	0	13	1	1	0	1
1	1	1	14	1	1	1	0

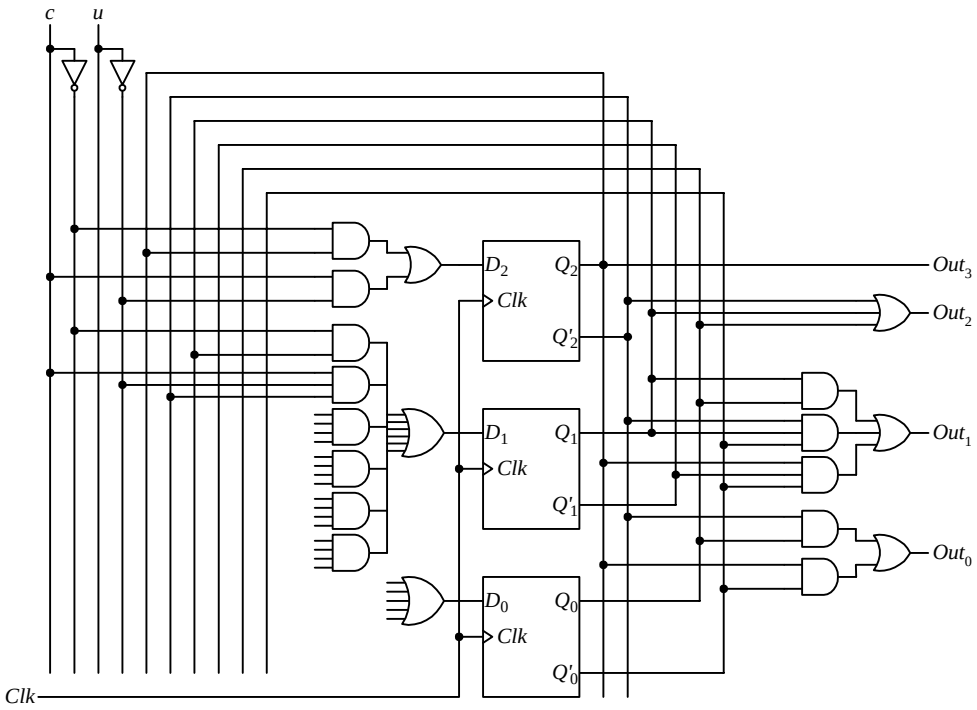
Output equations:

$Out_3 = Q_2$

$Out_2 = Q_2' + Q_1 + Q_0$

$Out_1 = Q_1Q_0 + Q_2'Q_1Q_0' + Q_2Q_1'Q_0'$

$Out_0 = Q_2'Q_0 + Q_2Q_0'$


c
u
D2
Q2
Clk
Q'2
D1
Q1
Clk
Q'1
D0
Q0
Clk
Q'0
Out3
Out2
Out1
Out0
Clk

3. Use a 4-bit up/down counter with parallel load to design a counter circuit that counts the following sequence repeatedly.

   54, 27, 39, 16, 8, 61 (6)

Answer

Counter will count 0, 1, 2, 3, 4, 5, 0, … for the six numbers in the sequence.
Use a decoder to convert the count to the needed number in the sequence.
Input to the decoder are the 4 bits from the counter.
The largest number to output is 61, therefore, the decoder output needs 6 bits since $2^6 = 64$.

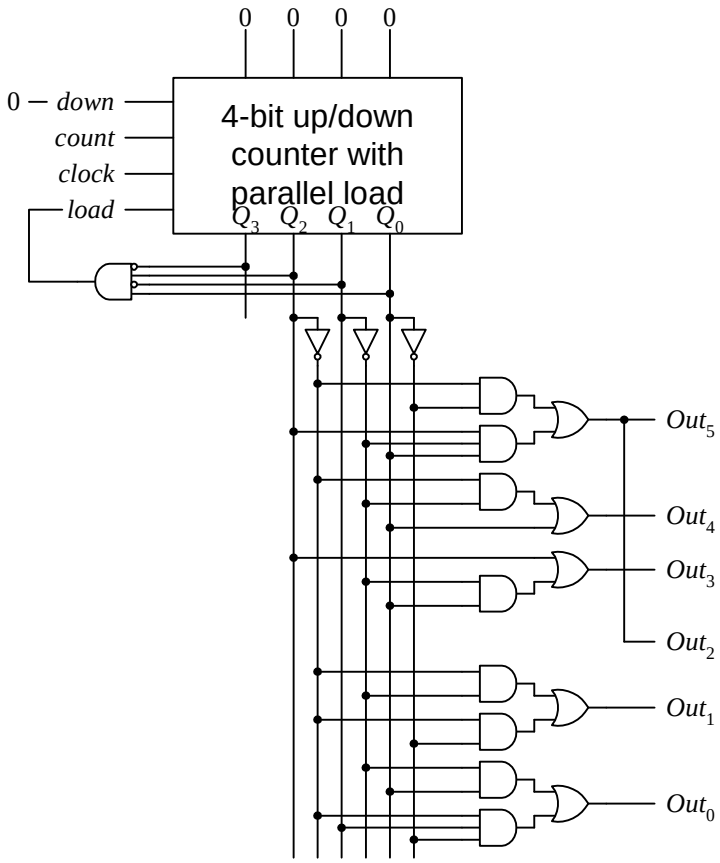
Decoder truth table:

Q_3	Q_2	Q_1	Q_0	Decimal	Out_5	Out_4	Out_3	Out_2	Out_1	Out_0
0	0	0	0	54	1	1	0	1	1	0
0	0	0	1	27	0	1	1	0	1	1
0	0	1	0	39	1	0	0	1	1	1
0	0	1	1	16	0	1	0	0	0	0
0	1	0	0	8	0	0	1	0	0	0
0	1	0	1	61	1	1	1	1	0	1
remaining					×	×	×	×	×	×

Output equations:

$Out_5 = Q_2'Q_0' + Q_2Q_1'Q_0$
$Out_4 = Q_2'Q_1' + Q_0$
$Out_3 = Q_2 + Q_1'Q_0$
$Out_2 = Out_5$
$Out_1 = Q_2'Q_1' + Q_2'Q_0'$
$Out_0 = Q_1'Q_0 + Q_2'Q_1Q_0'$

Circuit:


0 0 0 0
0
down
count
clock
load
4-bit up/down counter with parallel load
Q_3 Q_2 Q_1 Q_0
Out_5
Out_4
Out_3
Out_2
Out_1
Out_0