CS120B – Homework #2

Summer 2 2003. Professor Hwang

Given August 13, 2003. Due August 18, 2003 at the beginning of class.

No late homework accepted.

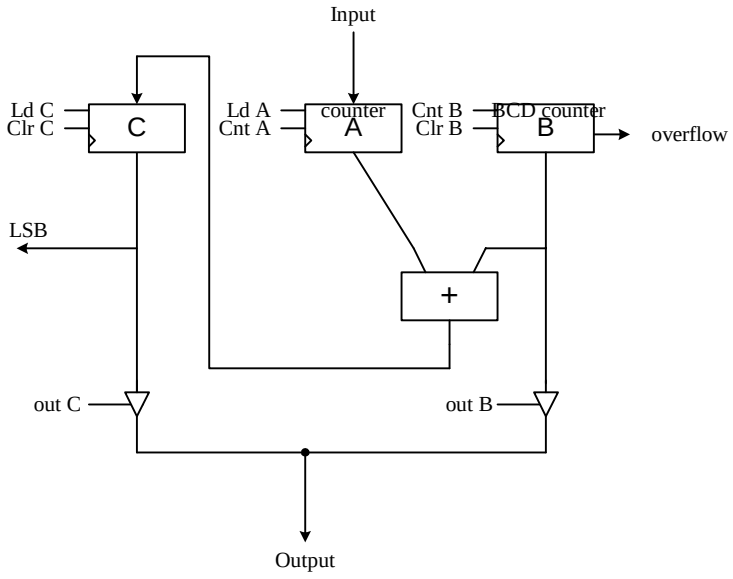
Your work must be completely typeset with a word processor. Circuit diagrams can be drawn using any drawing program or by hand but it must be very neat. Handwritten works will **NOT** be accepted. (13 points total)

1. Draw a datapath, using the fewest functional units that can execute the following algorithm. There should be only one data input port and one data output port.

```
Input A
C = 0
For B = 1 to 10 do
   C = A + B
   If C is odd then
      Output B
   Else
      A = A + 1
Output C
```

(3)

Answer



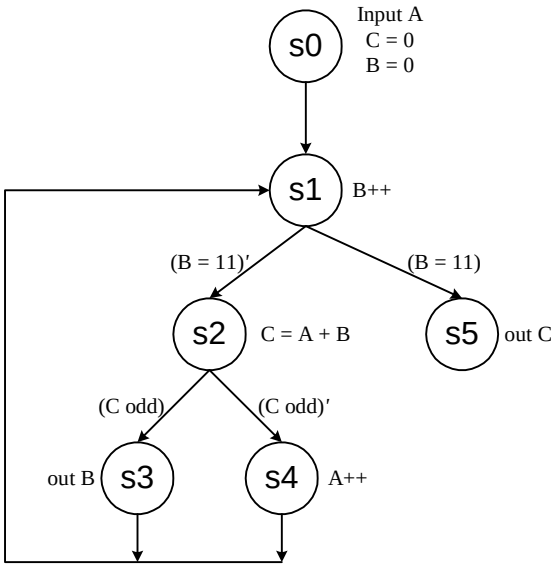
2. How many control signals is needed by your datapath for question 1? (1)

Answer

8 control signals

3. Draw the state diagram for a Moore FSM for the algorithm in question 1. (3)

Answer



4. Derive the control unit for the state diagram in question 3, using D flip-flops. (3)

Answer

Next-state table:

Current State $Q_2\ Q_1\ Q_0$	Next state $Q_{2next}\ Q_{1next}\ Q_{0next}$			
	(B=11), (C odd)			
	00	01	10	11
000	001	001	001	001
001	010	010	101	101
010	100	011	100	011
011	001	001	001	001
100	001	001	001	001
101	000	000	000	000
110	000	000	000	000
111	000	000	000	000

Implementation table:

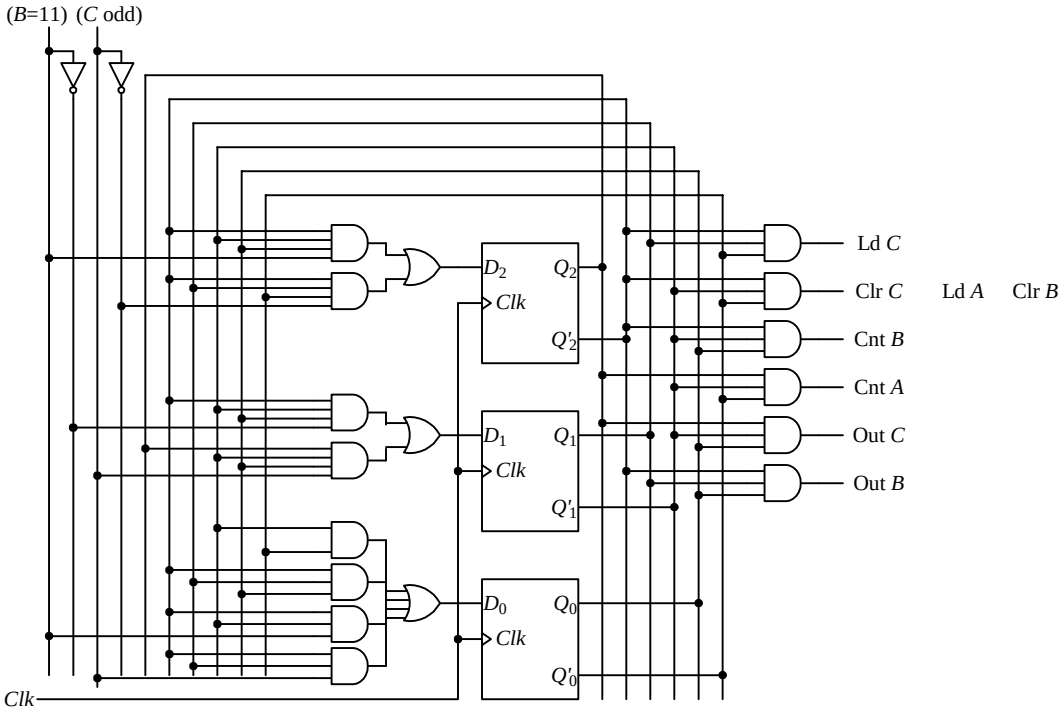
Current State $Q_2\ Q_1\ Q_0$	Implementation $D_2\ D_1\ D_0$			
	(B=11), (C odd)			
	00	01	10	11
000	001	001	001	001
001	010	010	101	101
010	100	011	100	011
011	001	001	001	001
100	001	001	001	001
101	000	000	000	000
110	000	000	000	000
111	000	000	000	000

$D_2 = Q_2'Q_1'Q_0(B{=}11) + Q_2'Q_1Q_0'(C \text{ odd})'$
$D_1 = Q_2'Q_1'Q_0(B{=}11)' + Q_2Q_1'Q_0(C \text{ odd})$
$D_0 = Q_1'Q_0' + Q_2'Q_1Q_0 + Q_2'Q_1'(B{=}11) + Q_2'Q_1(C \text{ odd})$

Output table:

	Ld C	Clr C	Ld A	Cnt A	Cnt B	Clr B	Out C	Out B
000	0	1	1	0	0	1	0	0
001	0	0	0	0	1	0	0	0
010	1	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	1
100	0	0	0	1	0	0	0	0
101	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0

Circuit:



5. Connect two 2K RAM chips to the 8051 such that the lowest location on one chip starts at memory address 0 hex and the lowest location on the second chip starts at 4K hex. (3)

Answer