

CS120B – Homework #1

Summer 2 2003. Professor Hwang

Given July 31, 2003. Due August 5, 2003 at the beginning of class.

No late homework accepted.

Your work must be completely typeset with a word processor. Circuit diagrams can be drawn using any drawing program or by hand but it must be very neat. Handwritten works will **NOT** be accepted. (12 points total)

1. Since we can use any of the four different types of flip-flops to synthesize the same functional circuit, we should, therefore be able to use one type of flip-flop to implement the functional operation of another type of flip-flop. Use the JK flip-flop to implement the operations of the SR, D, and T flip-flops. In other words, synthesize the circuit for the SR, D and T flip-flops using only JK flip-flops. You need to have three different circuits, one for each type of the three flip-flops. (3)

Answer

SR next-state table:

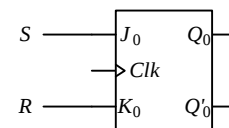
	SR=			
Q_0	00	01	11	10
0	0	0	$\times$	1
1	1	0	$\times$	1

$$J = S$$

$$K = R$$

SR implementation table using JK ff:

	SR=			
Q_0	00	01	11	10
0	$0\times$	$0\times$	$\times\times$	$1\times$
1	$\times 0$	$\times 1$	$\times\times$	$\times 0$



D next-state table:

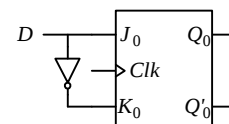
	D=	
Q_0	0	1
0	0	1
1	0	1

$$J = D$$

$$K = D'$$

D implementation table using JK ff:

	D=	
Q_0	0	1
0	$0\times$	$1\times$
1	$\times 1$	$\times 0$



T next-state table:

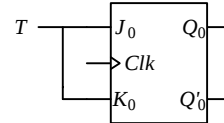
T implementation table using JK ff:

	T=	
Q_0	0	1
0	0	1
1	1	0

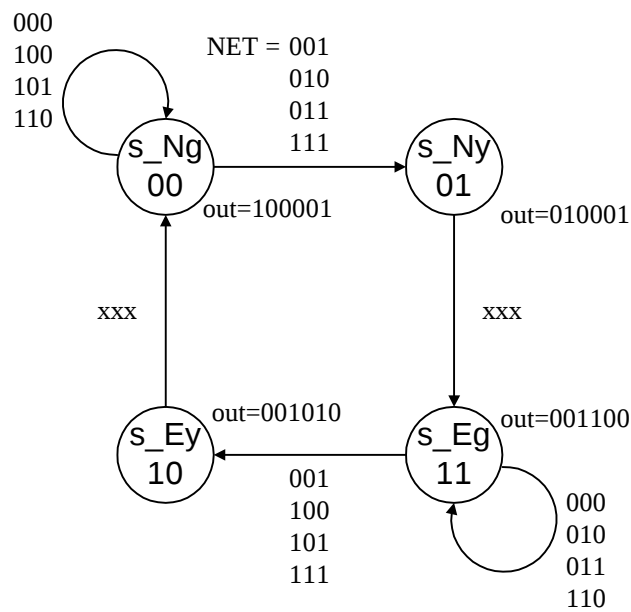
$$J = T$$

$$K = T$$

	T=	
Q_0	0	1
0	0×	1×
1	×	×



2. Synthesize a FSM for the following state diagram using SR flip-flops. The input bits are N, E, and T. The output bits are NSg, NSy, NSr, EWg, EWy, and EWr. (3)



Answer

Next-state table:

Current State $Q_1 Q_0$	Next State $Q_{1next} Q_{0next}$							
	NET=							
	000	001	010	011	100	101	110	111
00	00	01	01	01	00	00	00	01
01	11	11	11	11	11	11	11	11
11	11	10	11	11	10	10	11	10
10	00	00	00	00	00	00	00	00

Output table:

Current State $Q_1 Q_0$	Output $NSg, NSy, NSr, EWg, EWy, EWr$
00	100001
01	010001
11	001100
10	001010

$$NSg = Q_1'Q_0'$$

$$NSy = Q_1'Q_0$$

$$NSr = Q_1$$

$$EWg = Q_1Q_0$$

$$EWy = Q_1Q_0'$$

$$EWr = Q_1'$$

Implementation table:

Current State $Q_1 Q_0$	Implementation $S_1 R_1 S_0 R_0$							
	NET=							
	000	001	010	011	100	101	110	111
00	0×0×	0×10	0×10	0×10	0×0×	0×0×	0×0×	0×10
01	10×0	10×0	10×0	10×0	10×0	10×0	10×0	10×0
11	×0×0	×001	×0×0	×0×0	×001	×001	×0×0	×001
10	010×	010×	010×	010×	010×	010×	010×	010×

Excitation equations:

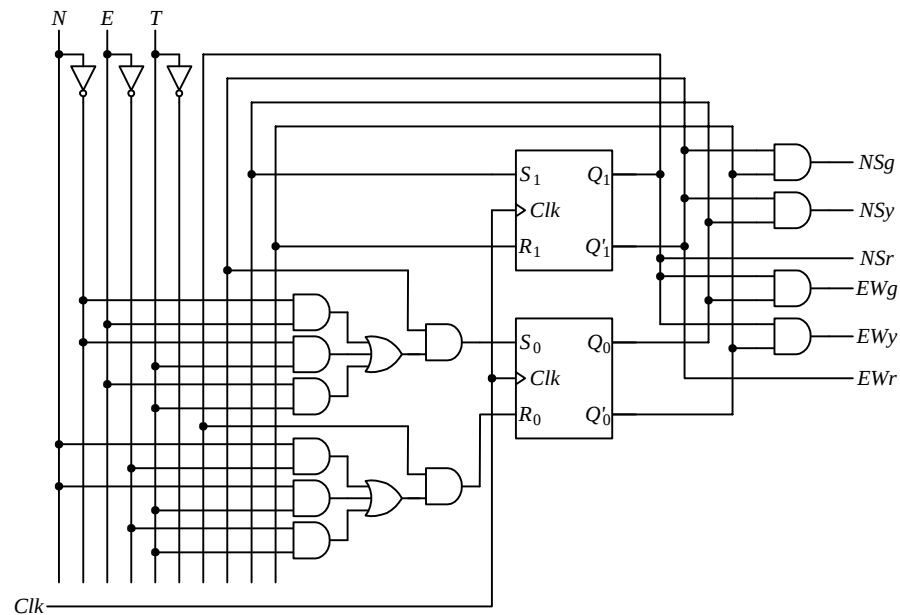
$$S_1 = Q_0$$

$$R_1 = Q_0'$$

$$S_0 = Q_1' (N' E + N' T + ET)$$

$$R_0 = Q_1 (NE' + NT + E' T)$$

Circuit:



3. Repeat question 2 but use T flip-flops.

(3)

Answer

Implementation table:

Current State $Q_1 Q_0$	Implementation							
	$T_1 T_0$							
	NET=							
	000	001	010	011	100	101	110	111
00	00	01	01	01	00	00	00	01
01	10	10	10	10	10	10	10	10
11	00	01	00	00	01	01	00	01
10	10	10	10	10	10	10	10	10

Excitation equations:

$$T_1 = Q_1 \oplus Q_0$$

$$T_0 = Q_1'Q_0'(N'T + N'E + ET) + Q_1Q_0(NE' + NT + E'T)$$

4. Repeat question 2 but use D flip-flops.

(3)

Answer

Implementation table:

Current State $Q_1 Q_0$	Implementation							
	$D_1 D_0$							
	NET=							
	000	001	010	011	100	101	110	111
00	00	01	01	01	00	00	00	01
01	11	11	11	11	11	11	11	11
11	11	10	11	11	10	10	11	10
10	00	00	00	00	00	00	00	00

Excitation equations:

$$D_1 = Q_0$$

$$D_0 = Q_1'Q_0 + Q_1'(N'T + N'E + ET) + Q_1(N'T' + N'E + ET')$$