

Name: Solution Key

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Student ID#:

(Numbers in parenthesis denote total possible points for question.)

1. Design a 4-bit up/down counter having the following operations using D flip-flops, HASs, and other necessary components. The control signals are *Load*, *E*, and *Down*. (4)

Load	E	Down	operation
0	0	×	no change
0	1	0	count up
0	1	1	count down
1	×	×	parallel load the input

Answer



- 2. Using a 4-bit up/down counter, design an up/down counter that counts as follows:
 - up: from 3 up to 7 and back to 3
 - down: from 5 down to 1 and back to 5

When the signal *Down* is changed, and the count is not within range of that count sequence, then the next count should start from the first number of that count sequence (3 for up and 5 for down). For example, assume that it is currently counting down. If *Down* changes when the count reaches 1, the next count is set to 3. (4)

Answer

The *Load* signal is asserted as follows:

- down: *Down* and (count = 1 or count > 5)
- up: Down' and (count = 7 or count < 3)



3. Synthesize a FSM that realizes the following state diagram using a JK flip-flop for the most significant bit and a D flip-flop for the least significant bit. (4)



Answer

Next-state / Output table

	Q_{1next}		
Q_1Q_0	C=0	C=1	Out
00	10	01	1
01	11	10	1
10	01	00	0
11	00	11	1

Implementation table

	$J_1 K_1$		
Q_1Q_0	C=0	C=1	Out
00	1×0	0×1	1
01	1×1	1×0	1
10	×11	×10	0
11	×10	×01	1

$$J_1 = C' + Q_0$$

$$K_1 = C' + Q_0'$$

$$D_0 = C \oplus Q_1 \oplus Q_0$$

$$Out = Q_1' + Q_0$$



4. Given the following memory circuit, determine all the possible addresses (in hex) to access locations 3 and 6 for both the top and bottom memory chip. (4)



Answer

Location	A_6	A_5	A_4	A ₃	A ₂	A_1	A ₀	Hex
Top 3	0	0	1	0	1	1	0	16
	1	0	1	0	1	1	0	56
Тор б	0	0	1	1	1	0	0	1C
	1	0	1	1	1	0	0	5C
Bottom 3	0	1	0	0	1	1	1	27
	1	1	0	0	1	1	1	67
Bottom 6	0	1	0	1	1	0	1	2D
	1	1	0	1	1	0	1	6D