CS120B – Homework #1

Given August 1, 2002. Due August 6, 2002 at the beginning of class.

1. How many bits wide is the data bus and the address bus on the (a) 8051; (b) Z80; (c) Pentium 4?

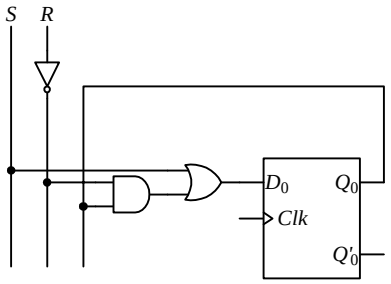
2. Since we can use any of the four different types of flip-flops to synthesize the same functional circuit, we should, therefore be able to use one type of flip-flop to implement the functional operation of another type of flip-flop. Use the D flip-flop to implement the operations of the SR, JK, and T flip-flops. In other words, synthesize the circuit for the SR, JK and T flip-flops using only D flip-flops. You need to have three different circuits, one for each type of the three flip-flops.

Answer

SR

	$Q_{0next} = D_0$ SR=			
Q_0	00	01	11	10
0	0	0	×	1
1	1	0	×	1

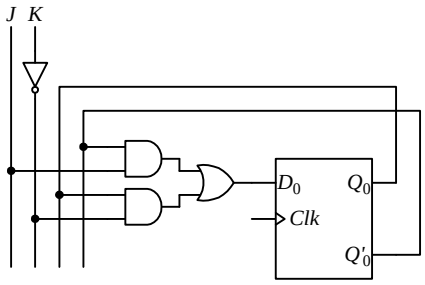
$D_0 = S + R'Q_0$



JK

	$Q_{0next} = D_0$ JK=			
Q_0	00	01	11	10
0	0	0	1	1
1	1	0	0	1

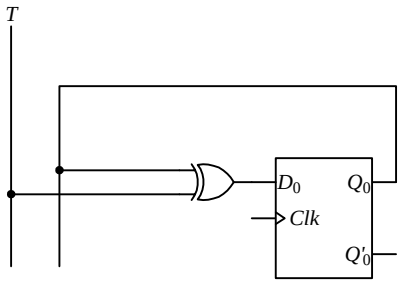
$D_0 = Q_0'J + Q_0K'$



T

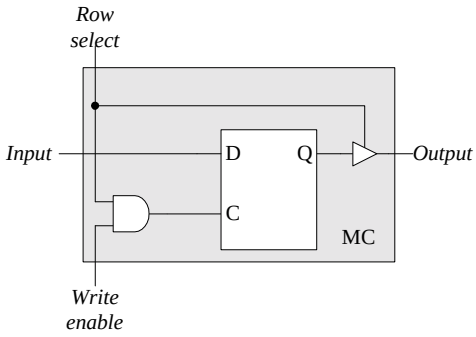
	$Q_{0next} = D_0$ T=	
Q_0	0	1
0	0	1
1	1	0

$D_0 = Q_0 \oplus T$

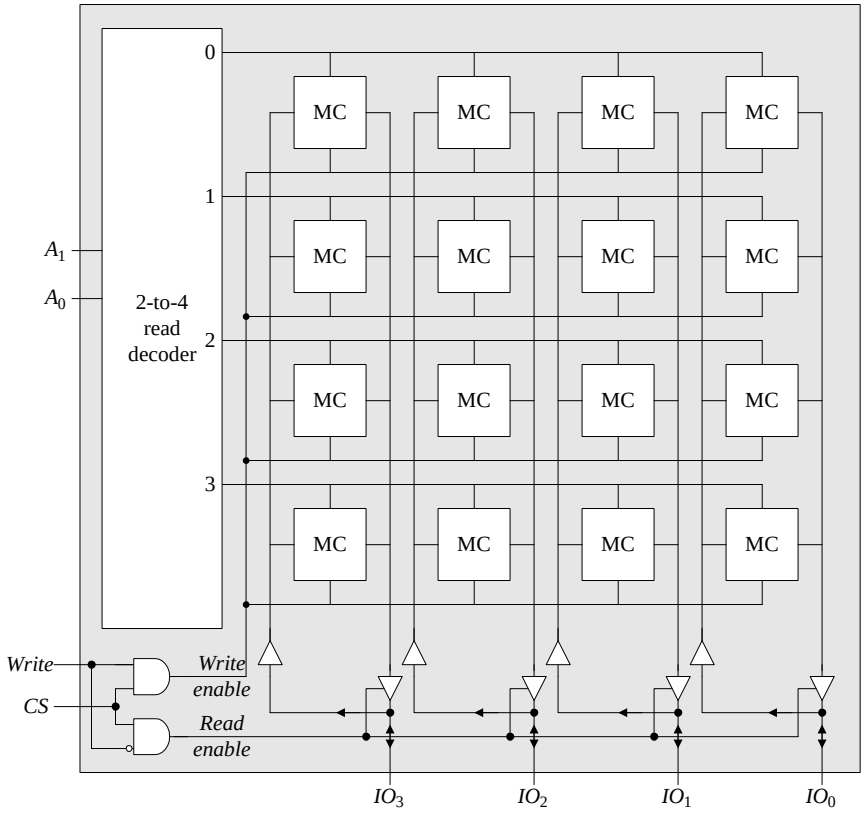


3. Regarding the memory cell circuit and the 4×4 RAM circuit that I gave in class, I said that there might be a problem since it might not retain its value when it is neither reading nor writing. Explain why or why not there is this problem. If there is this problem, then modify the circuit to correct it. Note that in the memory cell, a D-latch with enable is used (NOT a D-flipflop).

Answer



Memory Cell



4x4 RAM

There is nothing wrong with the above circuit. The D-latch with enable will retain its current value when *C* is de-asserted.