UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering
CS/EE120B – Introduction to Embedded Systems
Midterm 2
February 22, 2001

30

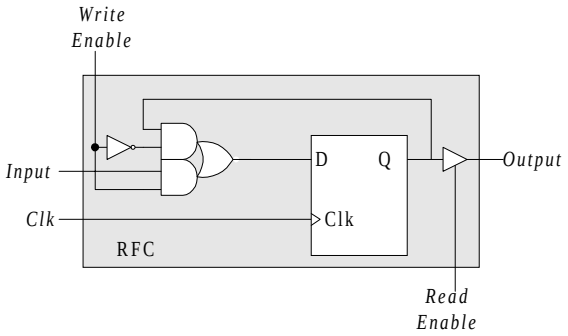
Name: Solution Key **Student ID#:** _____

Please print legibly

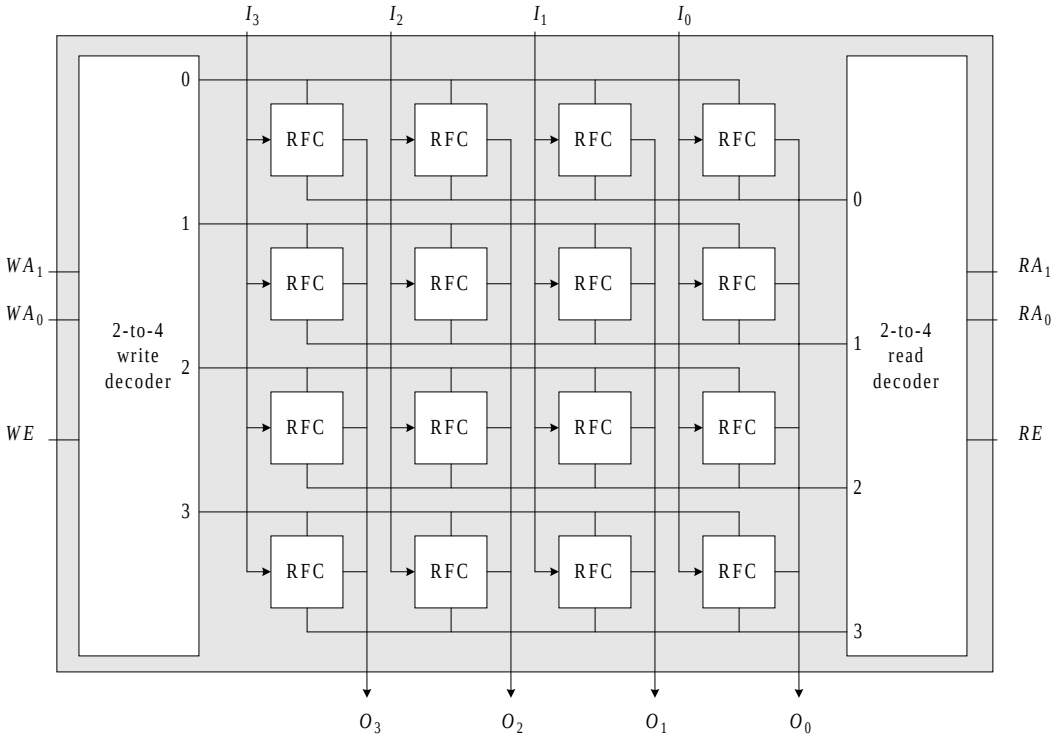
Lab Section: 21 (WF 6-10):____ **22** (MW 2-6):_____ **23** (TR 6-10):_____

(Numbers in parenthesis denote total possible points for question.)

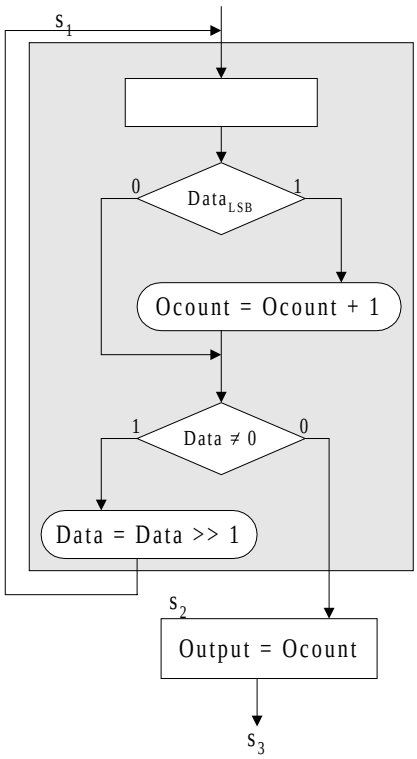
1. Given the following register file cell, draw the schematic for a 4-bit by 4-word register file with one 4-bit wide input port and one 4-bit wide output port. (5)

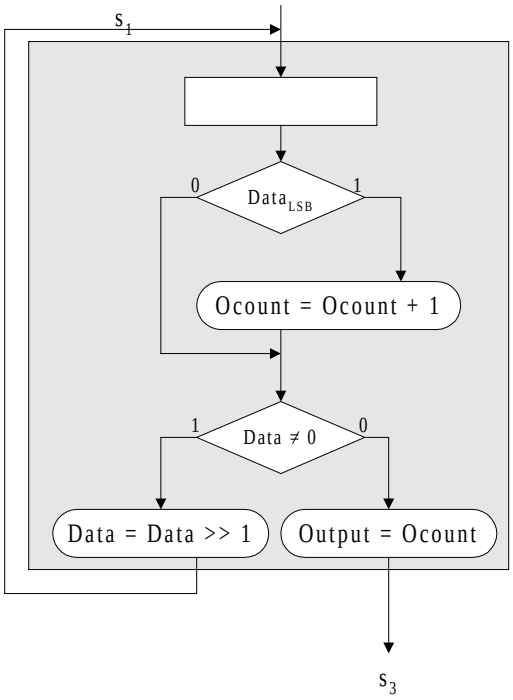


Answer


I_3
I_2
I_1
I_0
0
1
2
3
RFC
WA_1
WA_0
WE
2-to-4 write decoder
2-to-4 read decoder
RA_1
RA_0
RE
O_3
O_2
O_1
O_0

2. In the following incomplete ASM chart on the left, there are two states: s_1 and s_2. Can we move the unconditional assignment perform in s_2 into a conditional assignment box in s_1 as shown in the ASM chart on the right so that we don't need state s_2? Give your reasons. (5)

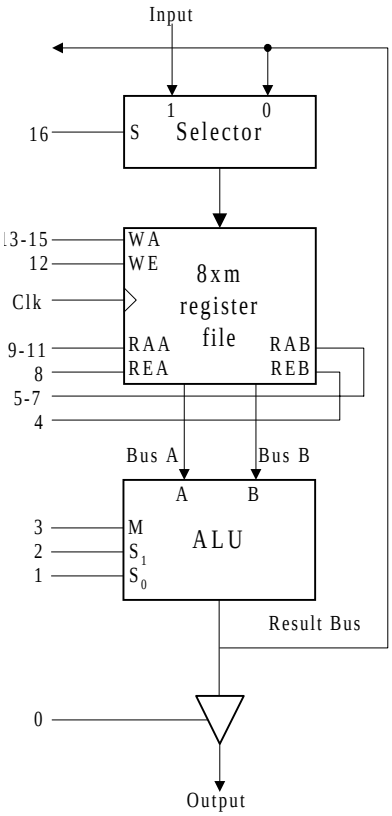




Answer

NO, we cannot move the unconditional assignment from s_2 to s_1 because the statement in s_2 reads the value of Ocount. However, Ocount is updated in s_1, and so if we read Ocount in s_1, it will be using the old value of Ocount and not the updated new value.

3. Using the following general datapath on the left and the ALU operations as defined on the right, write the control words required to implement the given pseudo code on the right. Your control words should be fully encoded to 0's, 1's, and don't cares, and not use any mnemonics. Don't cares should be used as much as possible. Register assignments should be in sequential order with first variable usage starting at R0. (5)



M	S_1	S_0	ALU operations
0	0	0	Set to 0
0	0	1	Set to 1
0	1	0	A AND B
0	1	1	Decrement B
1	0	0	A Multiply B
1	0	1	A Add B
1	1	0	A Subtract B
1	1	1	Pass B

ALU Functions

```
1  input n
2  product = 1
   while n > 1
3     product = product * n
4     n = n – 1
5  output product
```

Pseudo Code

Answer

Ctr	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Wd	IE	Write				Read A				Read B				ALU			OE
1	1	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	0
2	0	0	0	1	1	×	×	×	×	×	×	×	×	0	0	1	0
3	0	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	0
4	0	0	0	0	1	×	×	×	×	0	0	0	1	0	1	1	0
5	1	×	×	×	0	×	×	×	×	0	0	1	1	1	1	1	1

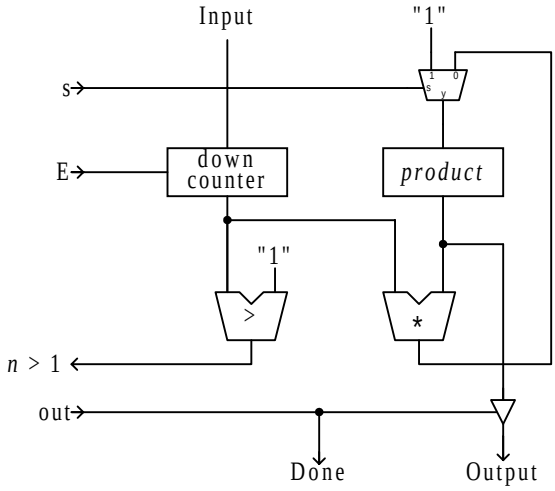
4. Design a custom datapath for a FSMD circuit for the following pseudo code. What is the minimum number of register(s) required and for which variable? What single functional units (i.e. not an ALU with multiple functions but single functional units such as an adder) are needed and for what operations? Draw the datapath. (7)

```
input n
product = 1
while n > 1
    product = product * n
    n = n – 1
output product
output done
```

Answer

The following registers and functional units are needed in the datapath:

- One register for variable *product*.
- One down counter for storing variable *n* and for decrementing *n*.
- One multiply functional unit.
- One greater-than-one comparator.



5. Design the Moore FSMD for the pseudo code below by constructing the state-action table only. Use as few states as possible. (8)

```
input n
product = 1
while n > 1
     product = product * n
     n = n – 1
output product
output done
```

Answer

State-action table for the Moore FSM

Current State $Q_2Q_1Q_0$ Name	Next State Condition, State	Control and Datapath Actions Actions
0 0 0 s_0	$\begin{bmatrix} Start = 0, s_0 \\ Start = 1, s_1 \end{bmatrix}$	$\begin{bmatrix} Done = 0 \\ Output = Z \end{bmatrix}$
0 0 1 s_1	s_2	$\begin{bmatrix} n = Input \\ Product = 1 \end{bmatrix}$
0 1 0 s_2	$\begin{bmatrix} n > 1, s_3 \\ n \le 1, s_4 \end{bmatrix}$	
0 1 1 s_3	s_2	*Product = Product * n* *n = n – 1*
1 0 0 s_4	s_0	*Output = Product*