UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering
CS/EE120B – Introduction to Embedded Systems
Midterm 1
January 30, 2000

30

Name: Solution Key **Student ID#:**
Please print legibly

Lab Section: 21 (WF 6-10):____ **22** (MW 2-6):_____ **23** (TR 6-10):_____

(Numbers in parenthesis denote total possible points for question.)

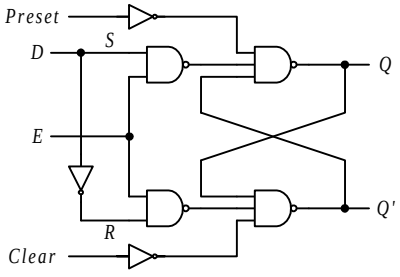
1. Briefly describe the *metastable behavior* of a bistable element. (3)

Answer

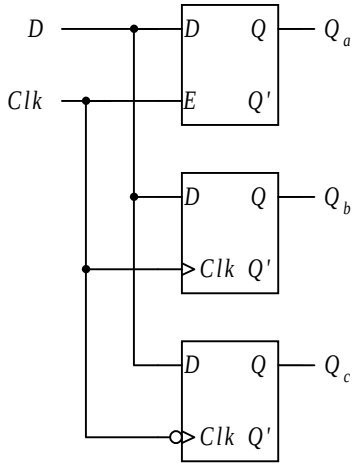
A bistable element has three (3) equilibrium points – Two are stable and the third is metastable. When a circuit is operating at the metastable point, it could theoretically stay there indefinitely if there is no noise whatsoever. However, with a small amount of noise, it will drive the circuit toward one of the two stable points.

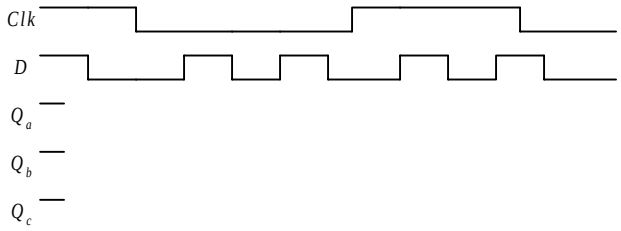
2. Use NAND gates and inverters to construct a D latch with active high enable, preset, and clear inputs. (5)

Answer

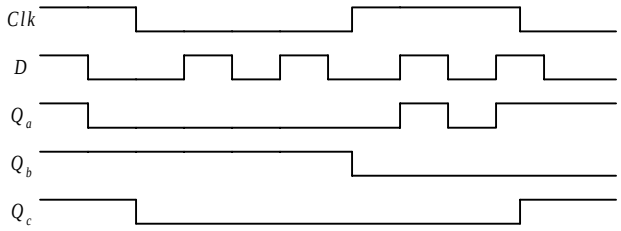


3. Complete the timing diagram below based on the following schematic (6)

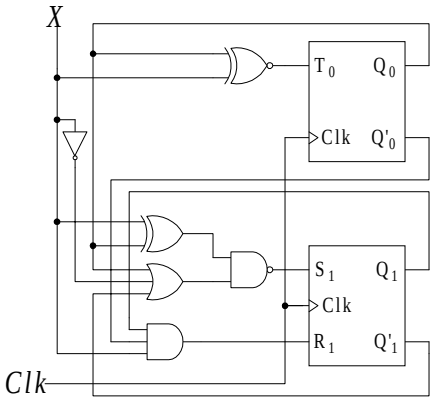




Answer



4. Derive the next state table and state diagram for the sequential circuit represented by the following schematic: (8)



Answer

Excitation equations:

$$T_0 = (X \oplus Q_0)' = X'Q_0' + XQ_0$$
$$S_1 = [(X \oplus Q_0)\,(X' + Q_1' + Q_0)]'$$
$$= (X \oplus Q_0)' + (X' + Q_1' + Q_0)'$$
$$= (X \oplus Q_0)' + (XQ_1Q_0')$$
$$R_1 = XQ_1Q_0'$$

Characteristic equations:

$$Q_{0next} = T_0 \oplus Q_0$$
$$Q_{1next} = S_1 + R_1'Q_1$$

Next state equations:

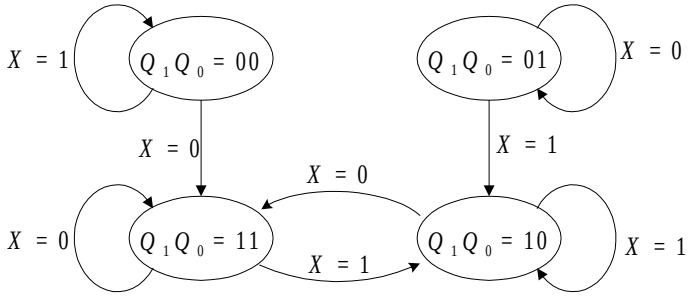
$$Q_{0next} = T_0 \oplus Q_0$$
$$= T_0Q_0' + T_0'Q_0$$
$$= (X'Q_0' + XQ_0)Q_0' + (XQ_0' + X'Q_0)Q_0$$
$$= X'Q_0' + X'Q_0$$
$$= X'$$

$$Q_{1next} = S_1 + R_1'Q_1$$
$$= (X \oplus Q_0)' + (XQ_1Q_0') + (XQ_1Q_0')'\,Q_1$$
$$= X'Q_0' + XQ_0 + (XQ_1Q_0') + (X' + Q_1' + Q_0)Q_1$$
$$= X'Q_0' + XQ_0 + (XQ_1Q_0') + X'Q_1 + Q_0Q_1$$

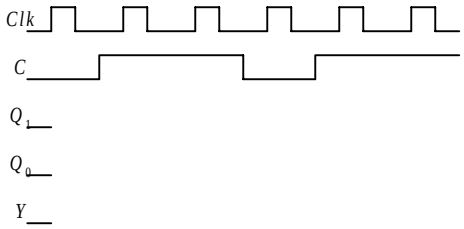
Next state table:

Current State Q_1Q_0	Next State $Q_{1next}\,Q_{0next}$	
	$X = 0$	$X = 1$
00	11	00
01	01	10
10	11	10
11	11	10

State diagram:



5. Synthesize a modulo-4 counter with a count enable input *C* and an output *Y* signal. The count is to be represented directly by the contents of two flip-flops; a JK flip-flop for the most significant bit and a T flip-flop for the least significant bit. Use the simple sequential binary encoding for the states. The counter counts when *C* is asserted and remains in the current state when *C* is de-asserted. The output *Y* is asserted when the count reaches 2 and the count enable input is enabled. Draw the synthesized circuit and complete the timing diagram below for the circuit. (8)



Answer