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CS/EE 120B
Homework #1 Given 1/18/01. Due 1/25/01

1. Using D flip-flops and basic gates, design a counter that counts in the following sequence: (8)

   1, 5, 6, 1, 5, 6, 1, 5, …

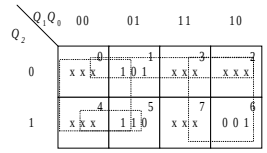
   The contents of the flip-flops are the binary equivalent of the count.

Answer

The next-state and transition tables for the counter could be defined as:

Q_2	Q_1	Q_0	Next-state
0	0	1	1 0 1
1	0	1	1 1 0
1	1	0	0 0 1

The K-map for the next-state table is:

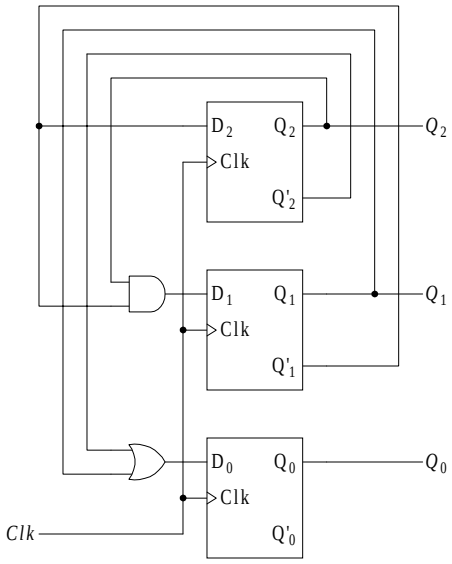


$Q_{2(next)}$, $Q_{1(next)}$, $Q_{0(next)}$
Next-state map.

The next-state equations are:

$D_2 = Q_{2(next)} = Q_1$'
$D_1 = Q_{1(next)} = Q_2\ Q_1$' or $Q_2\ Q_0$
$D_0 = Q_{0(next)} = Q_2$' + Q_1

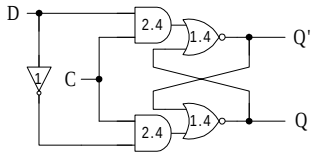
The schematic is as follows:

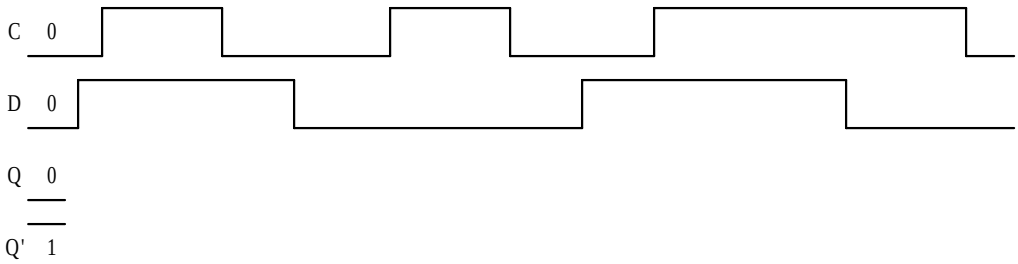


- ☞ 2 points for the next-state table.
- ☞ 2 points for the next-state equations.
- ☞ 4 points for getting the circuit correct.

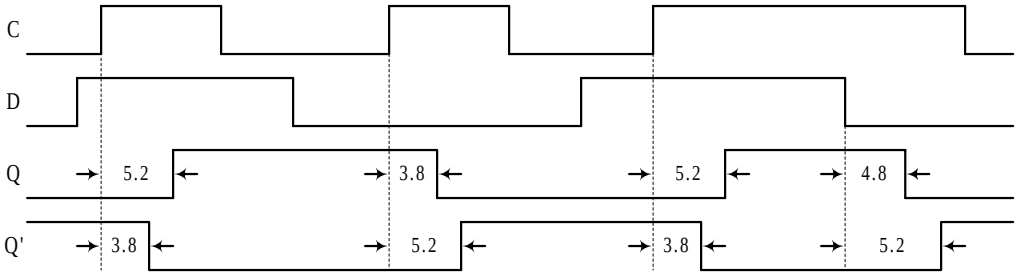
Total 8 points.

2. Given the following circuit for the D latch, complete the *Q* and *Q*' timing trace below. The initial values of *C*, *D*, *Q*, and *Q*' are given in the trace. Clearly label the delay times for all the changes for *Q* and *Q*' on the trace. The numbers written inside each gate in the circuit is the delay time for that gate. (8)



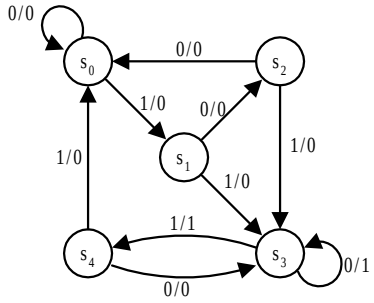


Answer



☞ 1 point each for getting one changing edge for *Q* or *Q*' and delay correct. Total 8 points.

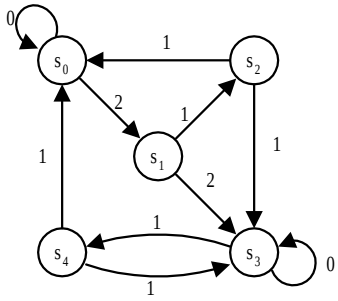
3. For the state diagram below, derive one possible best state encoding using the minimum-bit-change heuristic. What is the total edge weight for your encoding? (8)



Answer

Note that the input/output values on the edges are not used in this heuristic.
One possible state encoding is as follows:

s_0 = 100
s_1 = 010
s_2 = 110
s_3 = 111
s_4 = 101



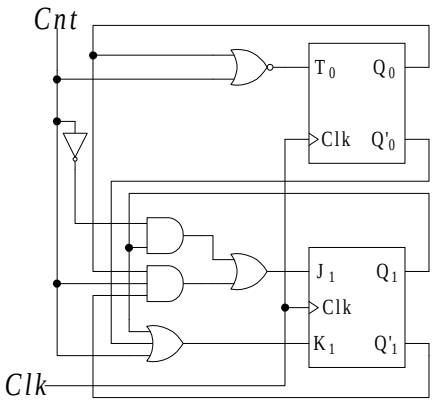
The total edge weight for this encoding is **10**.

Other encodings that will also give a total edge weight of 10:

s_0	100	101
s_1	000	001
s_2	001	000
s_3	010	011
s_4	110	111

- ☞ 5 points for getting a total edge weight of 10.
- ☞ 3 points for getting a total edge weight of 11

4. Derive the state table and state diagram for the sequential circuit represented by the following schematic:



(8)

Answer

Step 1: The excitation equations are: (2)

$$T_0 = (Cnt + Q_0)'$$
$$J_1 = Cnt'Q_1 + CntQ_1'Q_0$$
$$K_1 = Cnt + Q_1 + Q_0'$$

Step 2: The characteristic equation for the T flip-flop is:

Q_{next} = TQ' + T'Q = $T \oplus Q$

The characteristic equation for the JK flip-flop is:

Q_{next} = K'Q + JQ'

The next-state equations are: (2)

$$Q_{0next} = T_0 \oplus Q_0 = (Cnt + Q_0)' \oplus Q_0$$
$$= Cnt'Q_0' \oplus Q_0$$
$$Q_{1next} = K_1'Q_1 + J_1Q_1' = (Cnt + Q_1 + Q_0')'Q_1 + (Cnt'Q_1 + CntQ_1'Q_0)Q_1'$$
$$= Cnt'Q_1'Q_0Q_1 + Cnt'Q_1Q_1' + CntQ_1'Q_0$$
$$= 0 + 0 + CntQ_1'Q_0$$

Step 3a: The state table is: (2)

Present State	Next State	
Q_1Q_0	$Q_{1\,next}\,Q_{0\,next}$	
	$Cnt = 0$	$Cnt = 1$
00	01	00
01	01	11
10	01	00
11	01	01

Step 3b: The state diagram is: (2)