CS/EE 120B

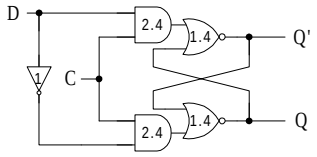
Homework #1 Given 1/18/01. Due 1/25/01

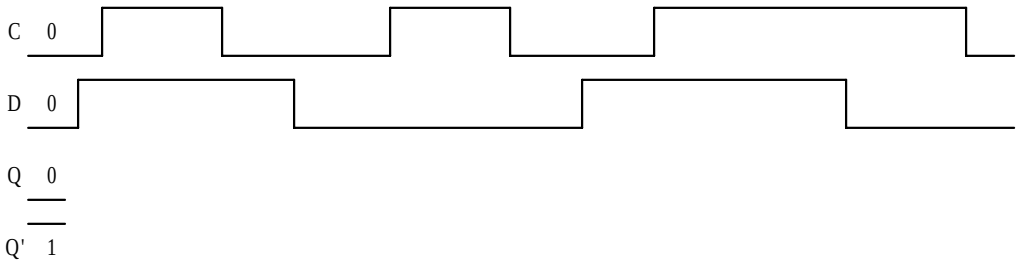
1. Using D flip-flops and basic gates, design a counter that counts in the following sequence:

   1, 5, 6, 1, 5, 6, 1, 5, …

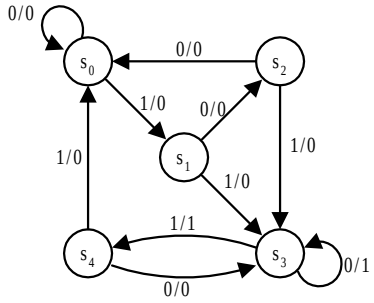
   The contents of the flip-flops are the binary equivalent of the count.

2. Given the following circuit for the D latch, complete the *Q* and *Q*' timing trace below. The initial values of *C*, *D*, *Q*, and *Q*' are given in the trace. Clearly label the delay times for all the changes for *Q* and *Q*' on the trace. The numbers written inside each gate in the circuit is the delay time for that gate.





3. For the state diagram below, derive one possible best state encoding using the minimum-bit-change heuristic. What is the total edge weight for your encoding?



4. Derive the state table and state diagram for the sequential circuit represented by the following schematic: