UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering

Department of Electrical Engineering

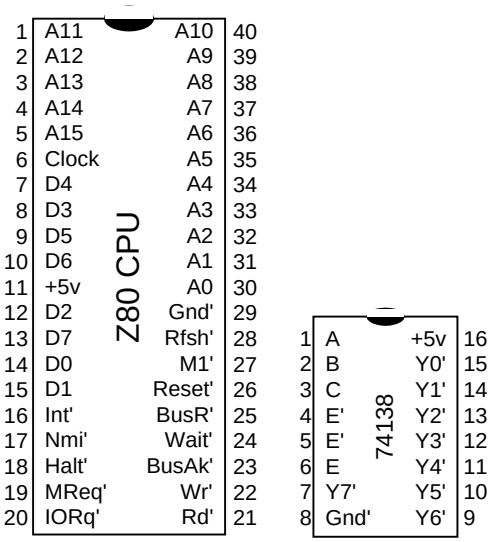
CS/EE120B – Logic Design

Homework 3

Given May 30, Due June 8, 2001

10

1. Draw the circuit schematic to interface the Z80 CPU with the RTC-62421 real-time clock module. Your schematic must be drawn with a computer drawing or CAD program. The pins for all chips in your schematic must be clearly label with both the pin number and the pin name. Connect the RTC so that it is accessed as an I/O device and its first register address at 80 hex. You must use the following three ICs. The datasheet and pin-outs for the RTC, Z80, and 74LS138 decoder are shown below.



The 74LS138 is a 3-to-8 decoder with three enable pins. A, B, & C are the input pins. Y0 to Y7 are the output pins. The three E pins are the enable pins. Note that some are active high and some are active low.

National Semiconductor

June 1989

54LS138/DM54LS138/DM74LS138, 54LS139/DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

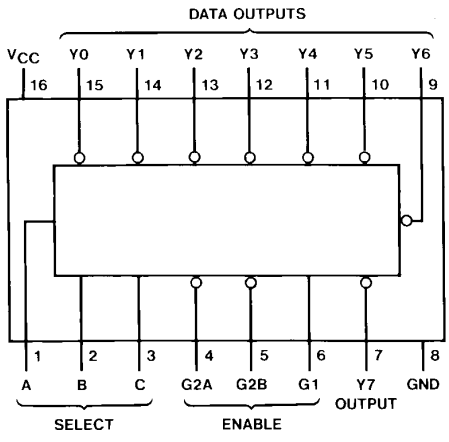
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

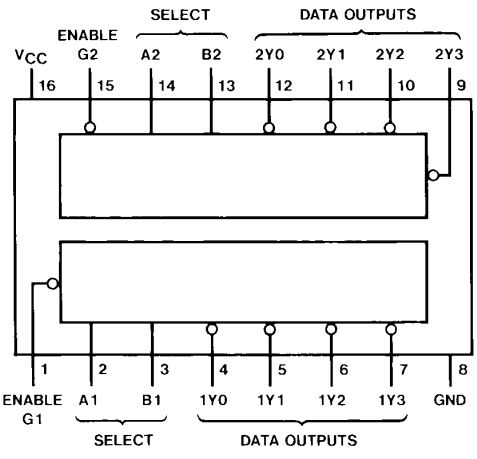
Dual-in-Line Package



TL/F/6391–1

Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-in-Line Package



TL/F/6391–2

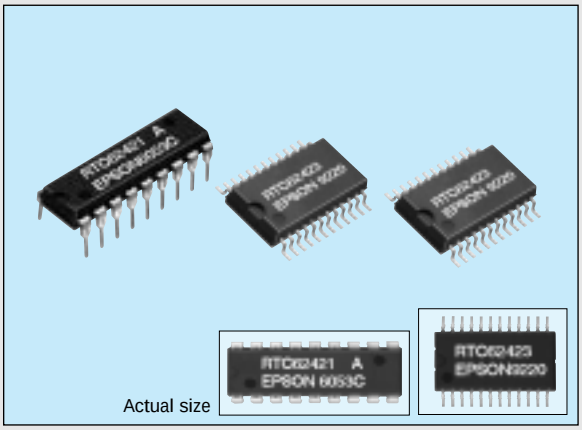
Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See NS Package Number E20A, J16A, M16A, N16E or W16A

RRD-B30M105/Printed in U. S. A.

4-bit REAL TIME CLOCK MODULE

RTC-62421/62423

- Built-in crystal unit allows adjustment-free efficient operation.
- Low standby voltage and current consumption (1.8µA at 2V).
- Wide range of operating temperature (from -40˚C to +85˚C).
- 24H/12H changeable and leap year automatically adjustable (gregorian calendar).
- Similar mounting method (RTC-62423) to that used for universal type SMD IC.
- Pins and functions are compatible with the MSM6242 series.



Specifications (characteristics)

Absolute Max. rating

Item	Symbol	Condition	Specifications	Unit
Power source voltage	V_{DD}	Ta=25˚C	-0.3 to 7.0	V
Input and output voltage	$V_{I/O}$		-0.3 to V_{DD}+0.3	
Storage temperature	T_{STG}	RTC-62421	-55 to +85	˚C
		RTC-62423	-55 to +125	
Soldering condition	T_{SOL}	RTC-62421	Under 260˚C within 10 sec. (lead part) (package should be less than 150˚C)	
		RTC-62423	Twice at under 260˚C within 10 sec. or under 230˚C within 3 min.	

Operating range

Item	Symbol	Condition	Specifications	Unit
Operating voltage	V_{DD}		4.5 to 5.5	V
Operating temperature	T_{OPR}		-40 to +85	˚C
Data holding voltage	V_{DH}		2.0 to 5.5	V
CS_1 data holding time	t_{CDR}	Refer to the data holding timing	2.0 min.	µs
Operation restoring time	t_R			

Frequency characteristics and current consumption characteristics

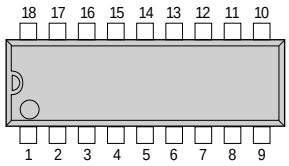
Item	Symbol	Condition		Specifications	Unit
Frequency tolerance	Δf/fo	Ta=25˚C V_{DD}=5V	62421 A	±10	ppm
			62421 B	±50	
			62423 A	±20	
			62423	±50	
Frequency temperature characteristics		-10 to +70˚C (25˚C reference temperature)		+10/-120	
		-40 to +85˚C (25˚C reference temperature)		+10/-220	
Aging	fa	V_{DD}=5V, Ta=25˚C, first year		±5 max.	ppm/y
Shock resistance	S.R.	Three drops on a hard board from 75 cm or 3000G x 0.3ms x 1/2 sine wave x 3 directions		±10 max.	ppm
Current consumption	I_{DD1}	CS_1=0V	V_{DD}=5V	30 max.	µA
	I_{DD2}		V_{DD}=2V	1.8 max.	

Electrical characteristics

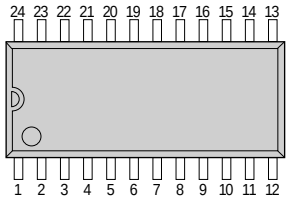
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable terminal
"H" input voltage (1)	V_{IH1}	—	2.2	—	—	V	All inputs other than CS_1
"L" input voltage (1)	V_{IL1}		—		0.8		
Input leak current (1)	I_{LK1}	V_I=V_{DD}/0V	—	—	1/-1	µA	Input other than D_0 to D_3
Input leak current (2)	I_{LK2}				10/-10		D_0 to D_3
"L" output voltage (1)	V_{OL1}	I_{OL}=2.5mA			0.4	V	
"H" output voltage	V_{OH}	I_{OH}=-400µA	2.4		—		
"L" output voltage (2)	V_{OL2}	I_{OL}=2.5mA	—		0.4		STD.P
OFF leak current	I_{OFFLK}	V_I=V_{DD}/0V			10	µA	
Input capacity	C_I	Input frequency 1 MHz		5	—	pF	
"H" input voltage (2)	V_{IH2}	V_{DD}=2 to 5.5V	4/5 V_{DD}	—	—	V	CS_1
"L" input voltage (2)	V_{IL2}		—		1/5 V_{DD}		

Terminal connection

RTC-62421



RTC-62423



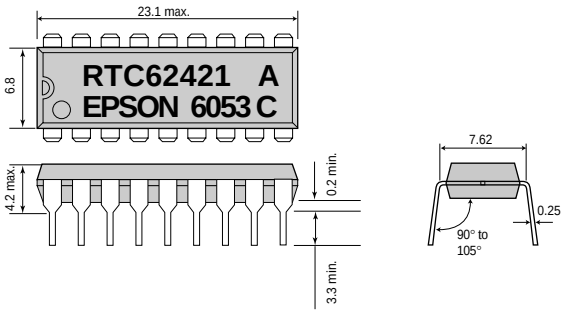
No.	62421	No.	62423
1	STD. P	1	STD. P
2	$\overline{CS_0}$	2	$\overline{CS_0}$
3	ALE	3	NC
4	A_0	4	ALE
5	A_1	5	A_0
6	A_2	6	NC
7	A_3	7	A_1
8	RD	8	NC
9	GND	9	A_2
10	$\overline{WR}$	10	A_3
11	D_3	11	RD
12	D_2	12	GND
13	D_1	13	$\overline{WR}$
14	D_0	14	D_3
15	CS_1	15	D_2
16	(V_{DD})	16	D_1
17	(V_{DD})	17	NC
18	V_{DD}	18	NC
		19	D_0
		20	CS_1
		21	NC
		22	(V_{DD})
		23	(V_{DD})
		24	V_{DD}

- (V_{DD}) and V_{DD} are to have the same level of voltage. Do not connect it to any external terminals.
- NC is not connected internally.

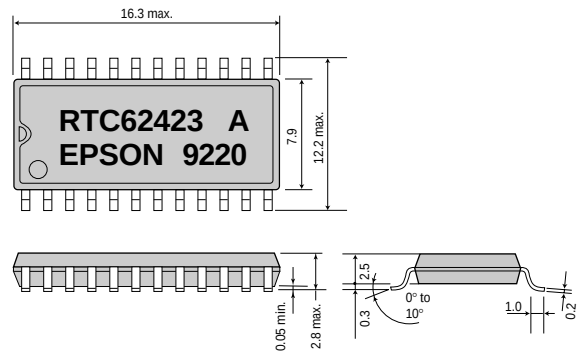
External dimensions

(Unit: mm)

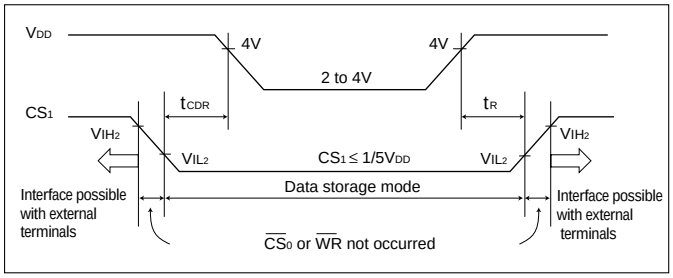
RTC-62421



RTC-62423



Data holding timing



Register table

Address	A3	A2	A1	A0	Name of register	D3	D2	D1	D0	Count	Note
0	0	0	0	0	S1	S8	S4	S2	S1	0 to 9	1 - sec. digit register
1	0	0	0	1	S10	*	S40	S20	S10	0 to 5	10 - sec. digit register
2	0	0	1	0	MI1	mi8	mi4	mi2	mi1	0 to 9	1 - min. digit register
3	0	0	1	1	MI10	*	mi40	mi20	mi10	0 to 5	10 - min. digit register
4	0	1	0	0	H1	h8	h4	h2	h1	0 to 9	1 - hour digit register
5	0	1	0	1	H10	*	PM/AM	h20	H10	0 to 2 or 0 to 1	10 - hour digit register
6	0	1	1	0	D1	d8	d4	d2	d1	0 to 9	1 - day digit register
7	0	1	1	1	D10	*		d20	d10	0 to 3	10 - day digit register
8	1	0	0	0	MO1	mo8	mo4	mo2	mo1	0 to 9	1 - month digit register
9	1	0	0	1	MO10	*			mo10	0 to 1	10 - month digit register
A	1	0	1	0	Y1	y8	y4	y2	y1	0 to 9	1 - year digit register
B	1	0	1	1	Y10	y80	y40	y20	y10		10 - year digit register
C	1	1	0	0	W	*	w4	w2	w1	0 to 6	Week register
D	1	1	0	1	CD	30 sec. ADJ	IRQ FLAG	BUSY	HOLD		Control register D
E	1	1	1	0	CE	t1	t0	ITRPT /STND	MASK		Control register E
F	1	1	1	1	CF	TEST	24/12	STOP	RESET		Control register F

Supplement

0="L" level. 1="H" level

	PM/AM	24/12	ITRPT/STND
1	PM	24	ITRPT
0	AM	12	STND

Bit name	Description
* mark	Writable. Recognized as 0 while in read mode.
BUSY	Read only (effective only when HOLD=1)
IRQ FLAG	Enter "0" only when clearing interruption. Enter "1" otherwise.
24H/12H	Set able only when RESET=1
TEST	For our company's testing. TEST should be "0" in normal use.

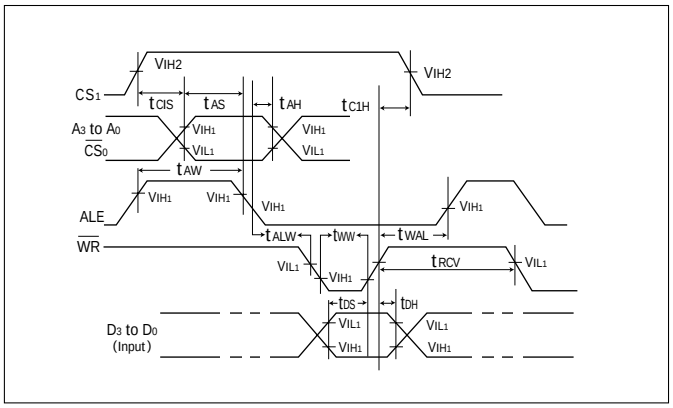
Note: Do not enter erroneous data for clock. This may result in time keeping error.

Switching characteristics

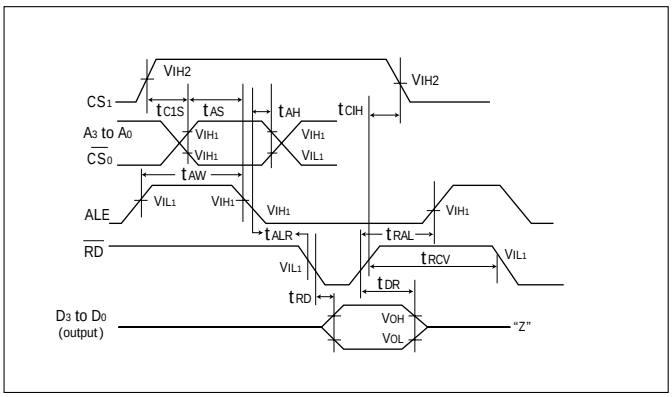
(VDD = 5V ± 0.5V, Ta = -40 to + 85°C)
(ALE = While in use)

Item	Symbol	Condition	Min.	Max.	Unit
CS1 setup time	tCIS		1000		
CS1 hold time	tCIH		1000		
Address setup time	tAS		25		
Address hold time	tAH		25		
ALE pulse width	tAW	—	40	—	
ALE before WRITE	tALW		10		
ALE before READ	tALR		10		
ALE after WRITE	tWAL		20		ns
ALE after READ	tRAL		10		
WRITE pulse width	tWW		120		
RD to data	tRD	CL=150pF		120	
DATA hold	tDR		0	45	
DATA setup time	tDS	—	100		
DATA hold time	tDH		10	—	
RD/WR recovery time	tRCV		60		

Write mode



Read mode



Block diagram