UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering
CS/EE120B – Introduction to Embedded Systems
Homework 1
Given April 9, 2001, Due April 18, 2001

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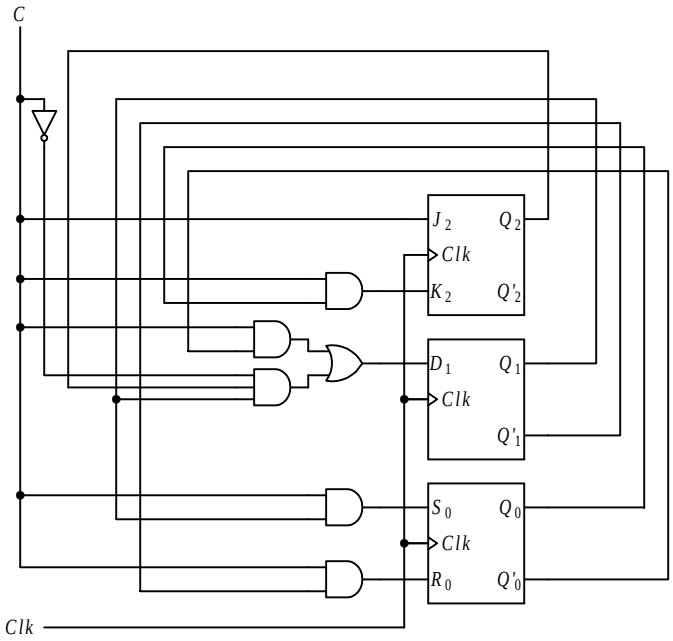
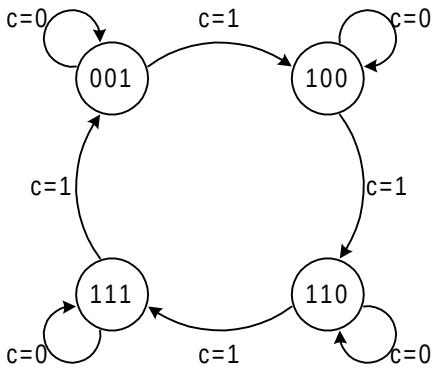
1. Derive the next-state/output table and state diagram for the following circuit. (5)



Answer

Current State $Q_2Q_1Q_0$	Next State $Q_{2next}\ Q_{1next}\ Q_{0next}$	
	$C = 0$	$C = 1$
001	001	100
100	100	110
110	110	111
111	111	001

3 points for getting this.



2 points for getting this

2. Synthesize a circuit that will count the following sequence using only one type of flip-flops:

   1, 4, 6, 7, 1, 4, 6, 7, ….

   The count is to be represented directly by the contents of the flip-flops. The counter is enabled by the input C. The count stops when $C = 0$. Determine which type of flip-flop (D, SR, JK, or T) gives the smallest circuit. You only need to draw the circuit using the flip-flops that gives the smallest circuit. Assume that the circuit size is proportional to the number of 2-input gates and inverters needed in the next-state function. (10)

Answer

The next-state table and D implementation table is:

Current State $Q_2Q_1Q_0$	Next State $Q_{2next}\ Q_{1next}\ Q_{0next}$	
	$C = 0$	$C = 1$
001	001	100
100	100	110
110	110	111
111	111	001

The equations are:

$D_2 = CQ_1' + C'Q_2 + Q_1Q_0'$
$D_1 = C'Q_1 + CQ_2Q_0'$
$D_0 = C'Q_0 + CQ_2Q_1$

Requires 13 2-input gates + 1 inverter

The SR implementation table is:

Current State $Q_2Q_1Q_0$	Implementation $S_2R_2\ S_1R_1\ S_0R_0$	
	$C = 0$	$C = 1$
001	0×0××0	100×01
100	×00×0×	×0100×
110	×0×00×	×0×010
111	×0×0×0	0101×0

The equations are:

$S_2 = CQ_2'$
$R_2 = CQ_2Q_0$
$S_1 = CQ_2Q_1'$
$R_1 = CQ_0$
$S_0 = CQ_1$
$R_0 = CQ_1$

Requires 8 2-input gates + 0 inverters

The JK implementation table is:

Current State $Q_2Q_1Q_0$	Implementation $J_2K_2\ J_1K_1\ J_0K_0$	
	$C = 0$	$C = 1$
001	0×0××0	1×0××1
100	×00×0×	×01×0×
110	×0×00×	×0×01×
111	×0×0×0	×1×1×0

+ 5 points for this

The equations are:

$J_2 = C$
$K_2 = CQ_0$
$J_1 = CQ_2$
$K_1 = CQ_0$
$J_0 = CQ_1$
$K_0 = CQ_2'$

+ 2 points for this

Requires 4 2-input gates + 0 inverters

The T implementation table is:

Current State $Q_2Q_1Q_0$	Implementation $T_2T_1T_0$	
	$C = 0$	$C = 1$
001	000	101
100	000	010
110	000	001
111	000	110

The equations are:

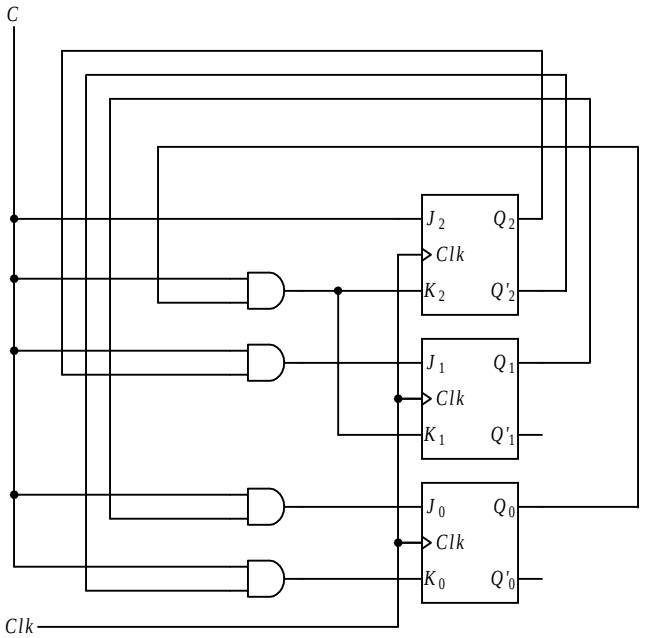
$T_2 = CQ_0$

$T_1 = CQ_2Q_1' + CQ_2Q_0$

$T_0 = CQ_2' + CQ_1Q_0'$

Requires 10 2-input gates + 0 inverters

<u>Using the JK flip-flop produces the smallest circuit size as shown below.</u>



+ 3 points for this. i.e.

only need this circuit to get full points.