UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering

CS/EE120B – Introduction to Embedded Systems
Final
Thursday June 14, 2001 8AM – 11AM

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Name: Solution Key________________ **Student ID#:**___________________
Please print legibly

Lab Section: 21 (TR 6-10):_____ **22** (WF 6-10):____ **23** (WF 2-6):_____

(Numbers in parenthesis denote total possible points for question.)

1. Discuss whether a flip-flop can be used as an input port for a general microprocessor system if the output of a flip-flop is connected directly to the system data bus. Give your reasons as to why it can or cannot be used. (4)

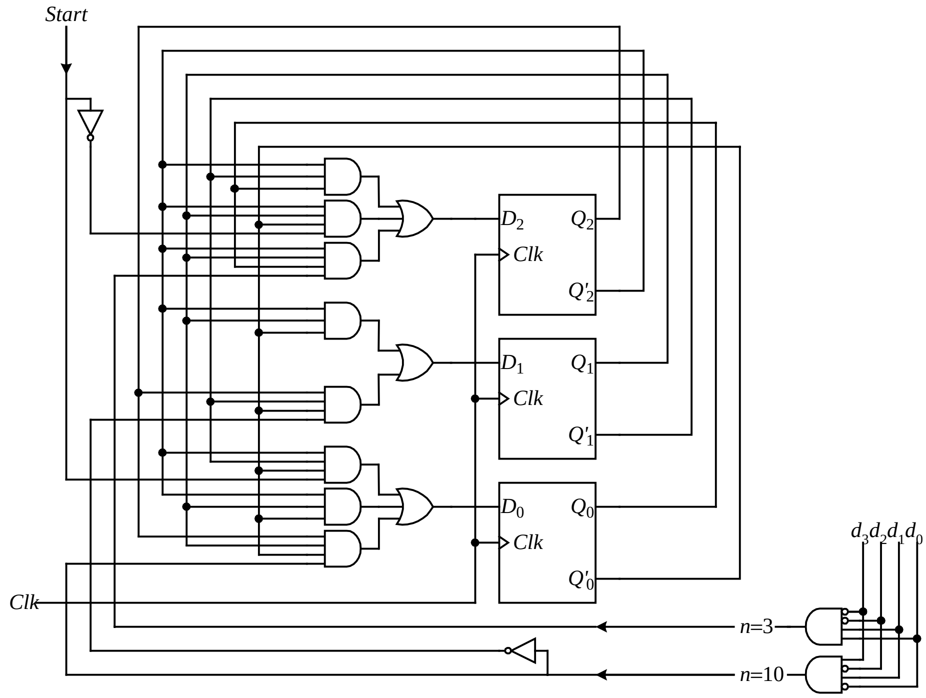
Answer

No. Since the flip-flop always outputs a value (0 or 1), the data bus is never released for other input devices to use. An input port requires a tri-state buffer where it can be disabled and outputs a "*Z*" value.

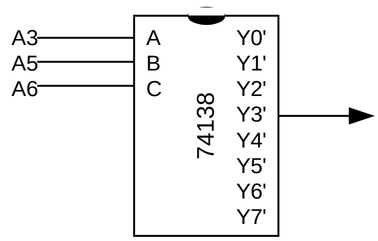
2. Draw the FSM using D flip-flops for the following next-state equations. The states are encoded using the straight sequential binary numbers. Using a 4-bit datapath, draw also the circuits to assert the required status signals used in the next-state equations. (4)

$$Q_{0next} = s_0 Start + s_2 + s_6(n = 10)$$
$$Q_{1next} = s_2 + s_4(n \neq 10)$$
$$Q_{2next} = s_1 + s_2 Start' + s_3(n = 3)$$

Answer



3. The following questions refer to the following 3-to-8 decoder circuit. Assume that the CPU that this circuit is connected to has 16 address lines (A0 to A15). Specify all addresses in hex. (4)



a) What is the lowest address (in hex) that will assert the output line Y_3?

b) What is the highest address (in hex) that will assert the output line Y_3?

c) What is the highest address (in hex) that will assert the output line Y_3 if A7 to A15 are all 0's?

d) Will the address 0AB7 (in hex) assert the output line Y_3? If no, then which output line will it assert?

Answer

011 for the three address lines A6, A5, and A3 will assert Y_3.
The lowest address will be when the rest of the address lines are 0.
The highest address will be when the rest of the address lines are 1.

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
a)	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
b)	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
c)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
d)	0	0	0	0	1	0	1	0	1	0	1	1	0	1	1	1

a) 0028 hex
b) FFBF hex
c) 003F hex
d) No, Y_2 is asserted because the three address bits A6,A5,A3 are 010.

4. Synthesize (construct) a JK flip-flop using a T flip-flop. i.e. construct a circuit using a T flip-flop and two inputs (J and K) to the circuit that has the same behavior (truth table) as the JK flip-flop. (4)

Answer

The JK truth table is

J	K	Q	Q_{next}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Re-write the JK truth table as a next-state table

	Q_{next}			
Q	JK = 00	JK = 01	JK = 11	JK = 10
0	0	0	1	1
1	1	0	0	1

The T excitation table is

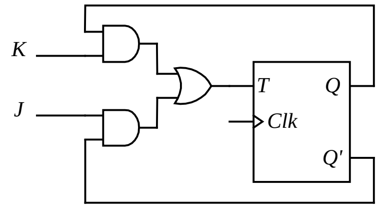
Q	Q_{next}	T
0	0	0
0	1	1
1	0	1
1	1	0

The implementation table is obtained by substituting the values from the T excitation table into the JK next-state table.

	T			
Q	JK = 00	JK = 01	JK = 11	JK = 10
0	0	0	1	1
1	0	1	1	0

From the T flip-flop implementation table, we get the following equation and circuit.

$$T = QK + Q'J$$



5. Which of the three datapaths shown below <u>cannot</u> be used to implement the following algorithm? Check all the datapaths that applies. For each datapath that you check, circle the extra or missing parts in the datapath that are wrong and give a brief reason as to why the datapath won't work. In the datapath schematics, all data lines are 8 bits and all signal lines are 1 bit except where noted. (4)

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sum = 0
input n
for i = 1 to n
    if (i mod 2) == 0
        sum = sum + 1
output sum
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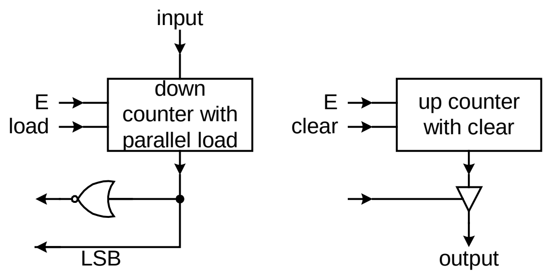
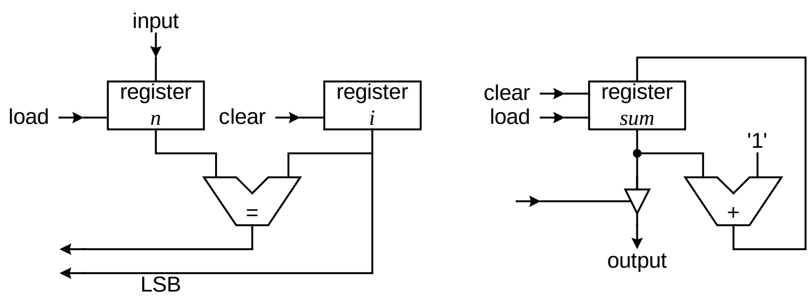
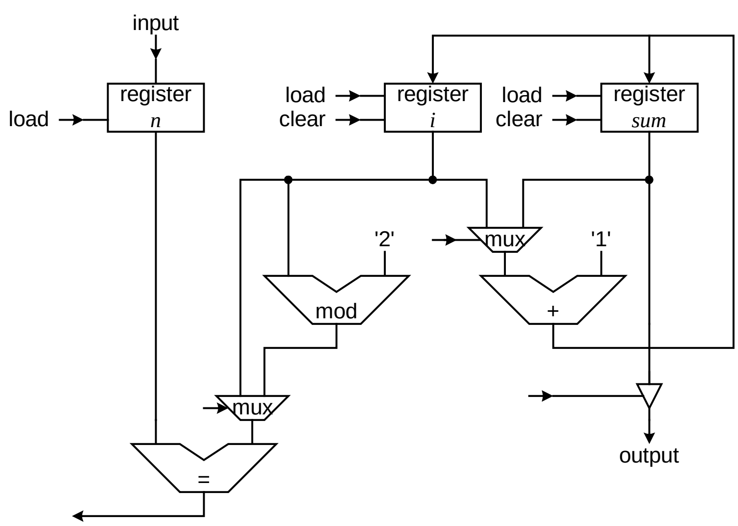
a)



b)



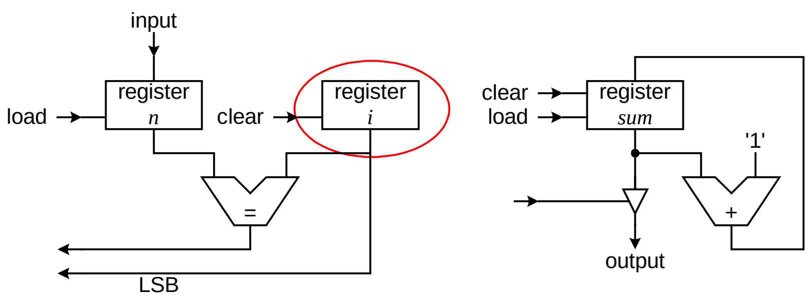
c)



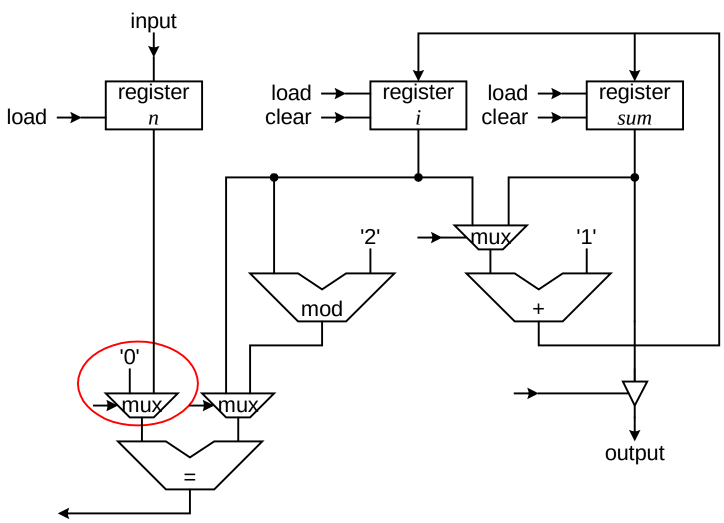
Answer

Datapaths b) and c) cannot implement the algorithm.

b) Can't increment *i*. Need a counter.



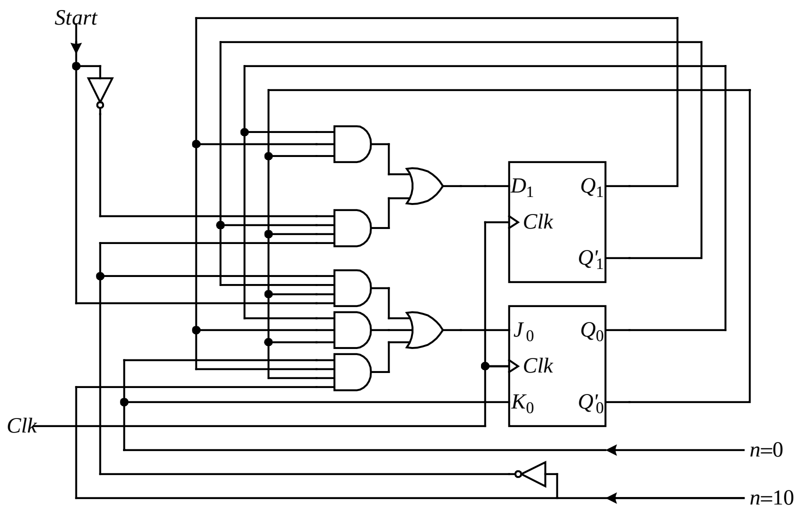
c) Can't compare (*i* mod 2) == 0. Need a mux and input a '0'.



Datapath a) can implement the algorithm as follows:

- The "down counter" can input *n* and count down to 1. When it counts down to 0, the NOR gate will assert the output. Thus, we don't need a register for *i*.
- Testing for mod 2 = 0 is the same as checking the LSB bit.
- *sum* is stored in the "up counter". The clear line will initialize *sum* to 0.
- The tri-state buffer will output *sum*.

6. Derive the state diagram for the following sequential circuit (4)



Answer

Excitation equations:

$D_1 = Q_1Q_0'Q_0 + Start'Q_1'Q_0'(n{=}10)'$
$\quad = Start'Q_1'Q_0'(n{=}10)'$
$J_0 = (n{=}10)'Q_1'Q_0'Start + Q_0Q_1Q_0' + (n{=}0)Q_1Q_0'(n{=}10)$
$\quad = (n{=}10)'Q_1'Q_0'Start$
$K_0 = (n{=}0)$

Characteristic equations:

$Q_{1next} = D_1$
$Q_{0next} = K_0'Q_0 + J_0Q_0'$

We get the next-state equations by substituting the excitation equations into the characteristic equations:

$Q_{1next} = D_1 = Start'Q_1'Q_0'(n{=}10)'$
$Q_{0next} = K_0'Q_0 + J_0Q_0'$
$\quad = (n{=}0)'Q_0 + (n{=}10)'Q_1'Q_0'StartQ_0'$
$\quad = (n{=}0)'Q_0 + (n{=}10)'Q_1'Q_0'Start$

Next-state table:

Current State Q_1Q_0	Next State *Start*, (n=0), (n=10)							
	000	001	010	011	100	101	110	111
00	00	00	00	00	10	00	10	00
01	01	01	00	00	01	01	00	00
10	00	00	00	00	00	00	00	00
11	01	01	00	00	01	01	00	00

State diagram: