Lab 6
ALU, Latch and Flip-Flop Design

Objectives

- To get familiar with the Xilinx VHDL Editor Tool.
- To design and implement simple combinational logic circuits using VHDL at the Structural level.
- Simulate and test combinational circuits.
- To download your circuit onto the prototype board and test it.

Laboratory Instructions

- Use the Xilinx VHDL editor to create the VHDL source file(s) for your design before coming to the lab.
- Create a directory with your name on drive C of your lab PC. Use this directory to create your project, store your results, bitsteams, etc. during the lab session.
- You can bring a complete project (i.e. *project.pdf* file and *project* directory) on a floppy disk and then use the **Copy Project** command from the Project Manager menu to copy it into the directory you created above.
- Alternatively, you can create a new project in your directory on the C drive and then copy your files to that new project directory. Remember to *Add* your VHDL file to the project.
- Perform functional simulation of your design and have it checked by your TA.
- If the circuit works as expected, implement it using the prototyping board assigned to you.
- Use keyboard and LEDs available to apply input stimuli and observe the outputs. Disconnect the XSPORT (parallel port) when you apply input stimulus from the workbench.
- Test and demonstrate your circuit to your TA.

Design Problems

Using the Xilinx VHDL Editor, design, test and demonstrate the following circuits. Your circuits should be as small as possible.

1. A 4-bit ALU circuit at the Behavioral level having the following functionalities:

   - The ALU should take in two 4-bit numbers.
   - Add the two numbers.
   - Subtract the two numbers.
   - Increment the first operand by 1.
   - Decrement the first operand by 1.
   - AND the two numbers.
   - OR the two numbers.
   - NAND the two numbers.
   - XOR the two numbers.
   - The output of the ALU consists of one 4-bit result and a carry/borrow bit.

   Note: when constructing the ALU, **do not** use LE's, AE's, and FA's as discuss in the lecture. All you really need are case statements, etc.

1. A SR Latch at the Structural level.

2. A D flip-flop with asynchronous active-low set and clear at the Behavioral level.