CS120A – Homework #3

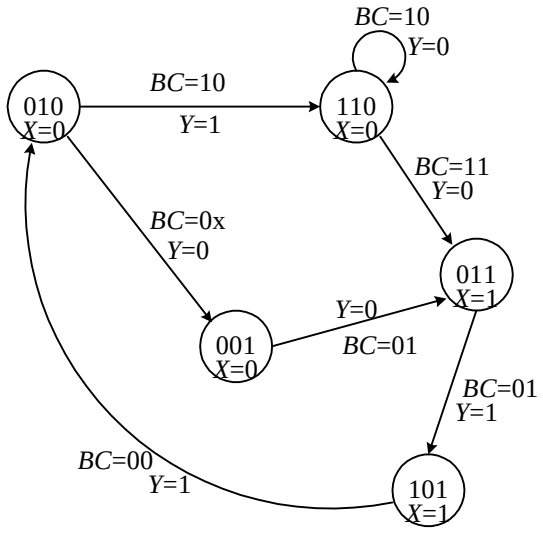
Spring 2003. Professor Hwang

Given May 29, 2003. Due June 5, 2003 at the beginning of class.

No late homework accepted.

Your work must be completely typeset with a word processor. Circuit diagrams can be drawn using any drawing program or by hand but it must be very neat. Handwritten works will **NOT** be accepted. (12 points total)

1. Synthesize a FSM for the following state diagram using D flip-flops. All equations must be minimized as much as possible taking all the "don't cares" into consideration. The variables *B* and *C* are inputs. The variables *X* and *Y* are outputs. (4)



Answer

Next-state / Output table:

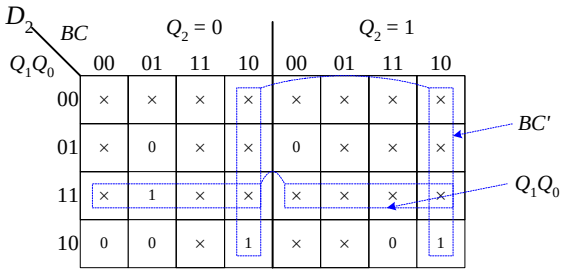
Current State	Next State / Output $Q_{2next}Q_{1next}Q_{0next}$ / Y				Output
	BC				X
$Q_2Q_1Q_0$	00	01	10	11	
000	××× / ×	××× / ×	××× / ×	××× / ×	×
001	××× / ×	011 / 0	××× / ×	××× / ×	0
010	001 / 0	001 / 0	110 / 1	××× / ×	0
011	××× / ×	101 / 1	××× / ×	××× / ×	1

100	××× / ×	××× / ×	××× / ×	××× / ×	×
101	010 / 1	××× / ×	××× / ×	××× / ×	1
110	××× / ×	××× / ×	110 / 0	011 / 0	0
111	××× / ×	××× / ×	××× / ×	××× / ×	×

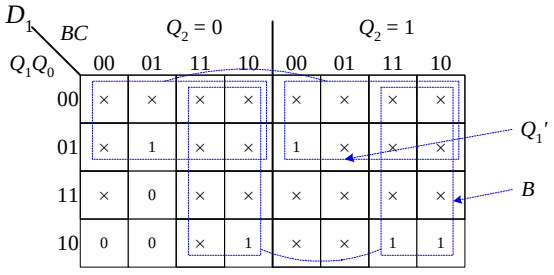
Implementation table:

Current State	Implementation $D_2D_1D_0$ / Y				Output
	BC				X
$Q_2Q_1Q_0$	00	01	10	11	
000	××× / ×	××× / ×	××× / ×	××× / ×	×
001	××× / ×	011 / 0	××× / ×	××× / ×	0
010	001 / 0	001 / 0	110 / 1	××× / ×	0
011	××× / ×	101 / 1	××× / ×	××× / ×	1
100	××× / ×	××× / ×	××× / ×	××× / ×	×
101	010 / 1	××× / ×	××× / ×	××× / ×	1
110	××× / ×	××× / ×	110 / 0	011 / 0	0
111	××× / ×	××× / ×	××× / ×	××× / ×	×

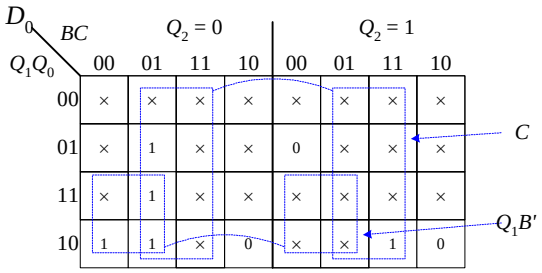
K-maps:



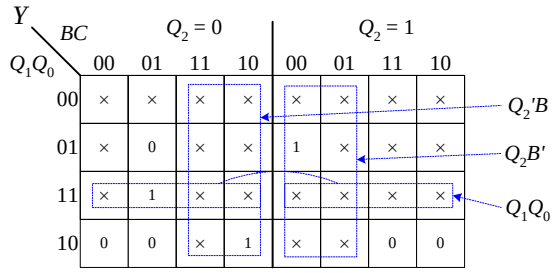
$D_2 = BC + Q_1Q_0$



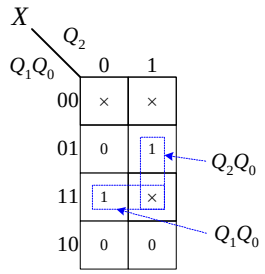
$D_1 = Q_1' + B$



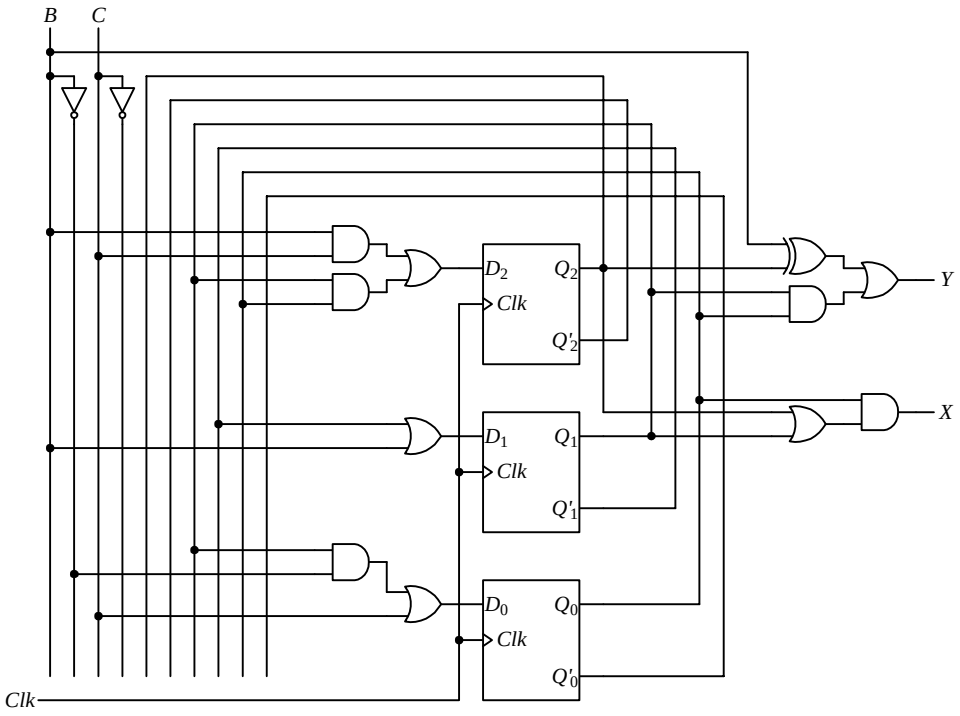
$$D_0 = Q_1B' + C$$



$$Y = Q_2'B + Q_2B' + Q_1Q_0 = (Q_2 \oplus B) + Q_1Q_0$$



$$X = Q_2Q_0 + Q_1Q_0 = Q_0(Q_2+Q_1)$$



2. Perform an analysis of the FSM circuit that you derived from question 1 above. Is the resulting state diagram the same as the original state diagram given in question 1? Explain your answer. (4)

Answer

Next-state equations:

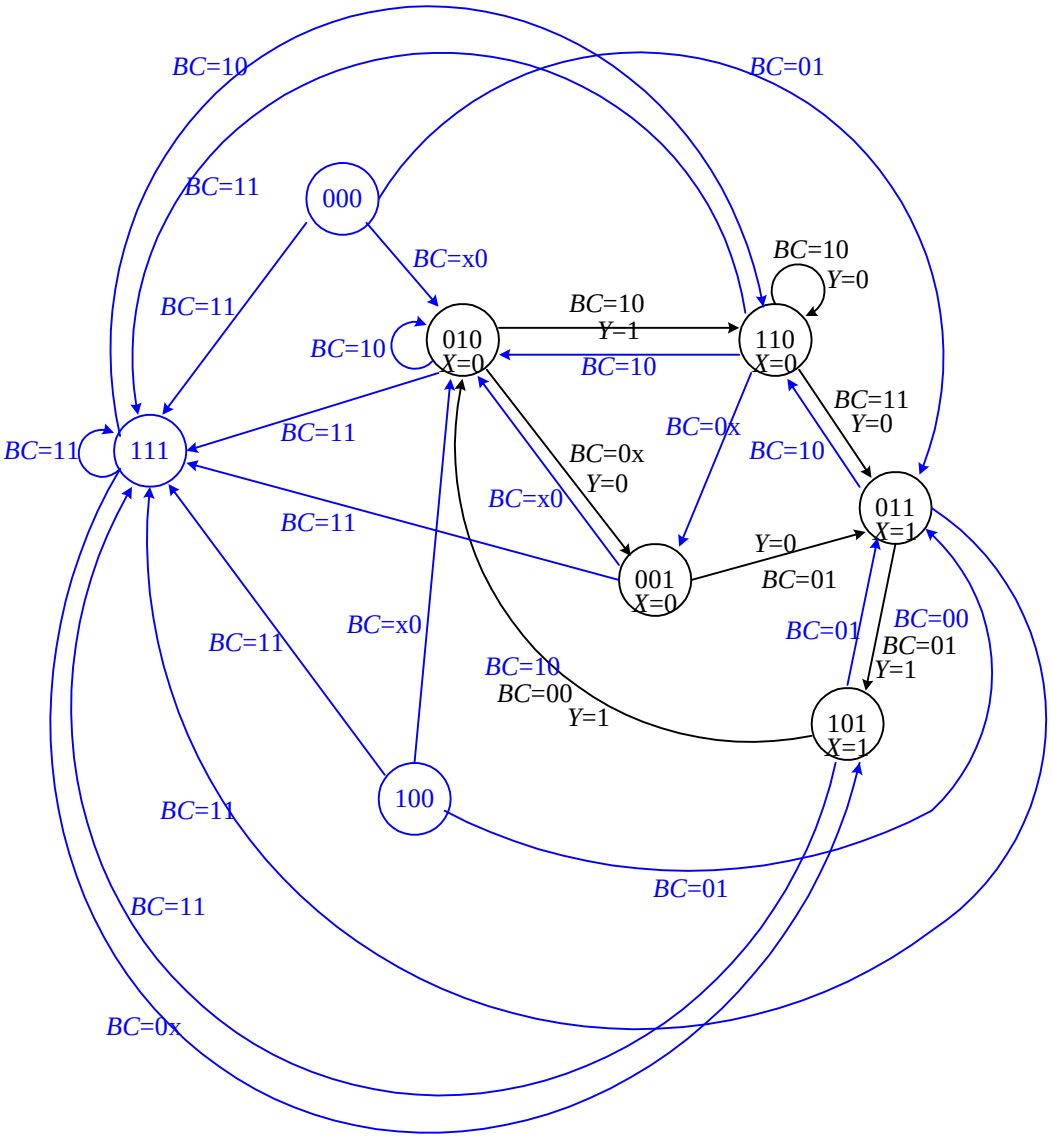
$Q_{2next} = D_2 = BC + Q_1Q_0$

$Q_{1next} = D_1 = Q_1' + B$

$Q_{0next} = D_0 = Q_1B' + C$

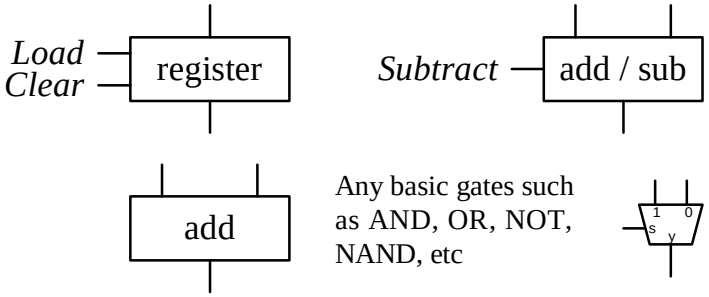
Next-state table:

Current State	Next State $Q_{2next}Q_{1next}Q_{0next}$			
	BC			
$Q_2Q_1Q_0$	00	01	10	11
000	010	011	010	111
001	010	011	010	111
010	001	001	010	111
011	101	101	110	111
100	010	011	010	111
101	010	011	010	111
110	001	001	010	111
111	101	101	110	111



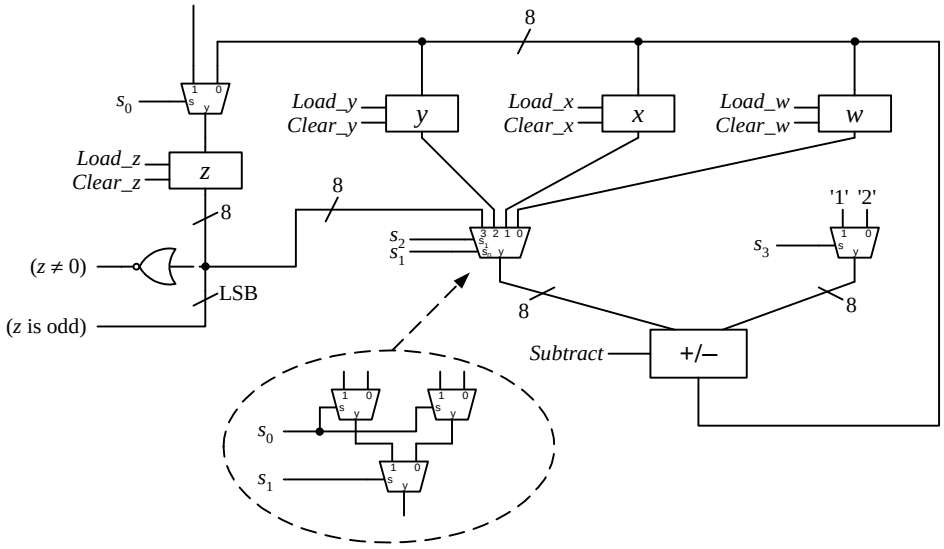
The two state diagrams are not the same because all the “don’t cares” from question 1 are now changed to the value 1. With no “don’t cares,” there are now eight nodes and all the nodes have four outgoing edges.

3. Use only the components given below to construct the smallest datapath that can execute the given algorithm below. You can use each component more than once, but you can only use the components given. The datapath width is 8-bits wide, i.e., the variables and registers are all 8 bits. How many control signals and status signals are there? (4)




```
w = 0
x = 0
y = 0
input z
while (z ≠ 0) {
   w = w – 2
   if (z is an odd number)
      x = x + 2
   else
      y = y + 1
   z = z – 1
   }
```

Answer



13 control signals and 2 status signals