UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering
CS/EE120A – Logic Design
Midterm 2
February 22, 2001

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Name: Solution Key **Student ID#:**_____
Please print legibly

Lab Section: 21 (MW 3-6):_____ **22** (TR 2-5):_____ **23** (MF 8-11):_____

(Numbers in parenthesis denote total possible points for question.)

1. Use the tabulation method to find the PI list and the EPI list for the function (5)

$$f = w'x'y'z' + xy'z + w'xz + wxy.$$

Answer

The 1-minterms are: m_0, m_5, m_7, m_{13}, m_{14}, m_{15}.
List of 0-subcubes:

Group ID	Subcube Minterms	Subcube Value				Subcube Covered
		w	x	y	z	
G_0	m_0	0	0	0	0	
G_2	m_5	0	1	0	1	yes
G_3	m_7	0	1	1	1	yes
	m_{13}	1	1	0	1	yes
	m_{14}	1	1	1	0	yes
G_4	m_{15}	1	1	1	1	yes

List of 1-subcubes:

Group ID	Subcube Minterms	Subcube Value				Subcube Covered
		w	x	y	z	
G_2	$m_{5,7}$	0	1	-	1	yes
	$m_{5,13}$	-	1	0	1	yes
G_3	$m_{7,15}$	-	1	1	1	yes
	$m_{13,15}$	1	1	-	1	yes
	$m_{14,15}$	1	1	1	-	

List of 2-subcubes:

Group ID	Subcube Minterms	Subcube Value				Subcube Covered
		w	x	y	z	
G_2	$m_{5,7,13,15}$	-	1	-	1	

The PI list is: xz , wxy, $w'x'y'z'$

Prime Implicant Name	Prime Implicant Expression	Implicant Minterms	Function Minterms					
			0	5	7	13	14	15
P_1	*xz*	(14,15)					⊗	×
P_2	*wxy*	(5,7,13,15)		⊗	⊗	⊗		×
P_3	*w'x'y'z'*	(0)	⊗					
	EPI covered minterms:		0	5	7	13	14	15
	Not covered minterms:							

The EPI list is: *xz* , *wxy*, *w'x'y'z'*

☞ 2 points if PI and EPI lists are obtained using K-maps.

2. Derive the minimized equations for the full subtractor circuit. Draw the full subtractor circuit using only 2-input basic gates (AND, OR, NOT, XOR) from the minimized equations. Your circuit should use as few gates as possible. (5)

Answer

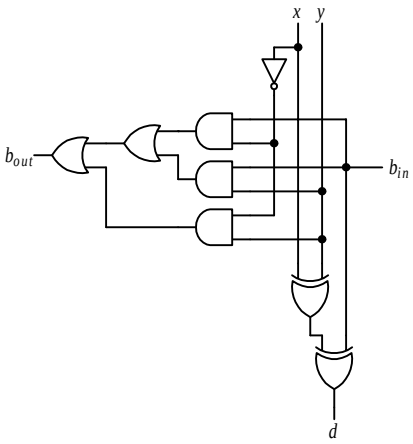
The full subtractor truth table is

b_{in}	x	y	b_{out}	d
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

Thus, the minimized equations are:

$$b_{out} = b_{in}x' + b_{in}y + x'y$$
$$d = b_{in} \oplus x \oplus y$$

The circuit is



3. Derive the equation for the carry lookahead signal c_3 in terms of the two operand inputs x and y, and c_0. (5)

Answer

$c_{i+1} = g_i + p_i c_i$

$$
\begin{aligned}
c_1 &= g_0 + p_0 c_0 \\
c_2 &= g_1 + p_1 c_1 \\
&= g_1 + p_1(g_0 + p_0 c_0) \\
&= g_1 + p_1 g_0 + p_1 p_0 c_0 \\
c_3 &= g_2 + p_2 c_2 \\
&= g_2 + p_2(g_1 + p_1 g_0 + p_1 p_0 c_0) \\
&= g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_0
\end{aligned}
$$

Substituting $g_i = x_i y_i$ and $p_i = x_i + y_i$ into c_3, we get

$$c_3 = x_2 y_2 + (x_2 + y_2) x_1 y_1 + (x_2 + y_2)(x_1 + y_1) x_0 y_0 + (x_2 + y_2)(x_1 + y_1)(x_0 + y_0) c_0$$

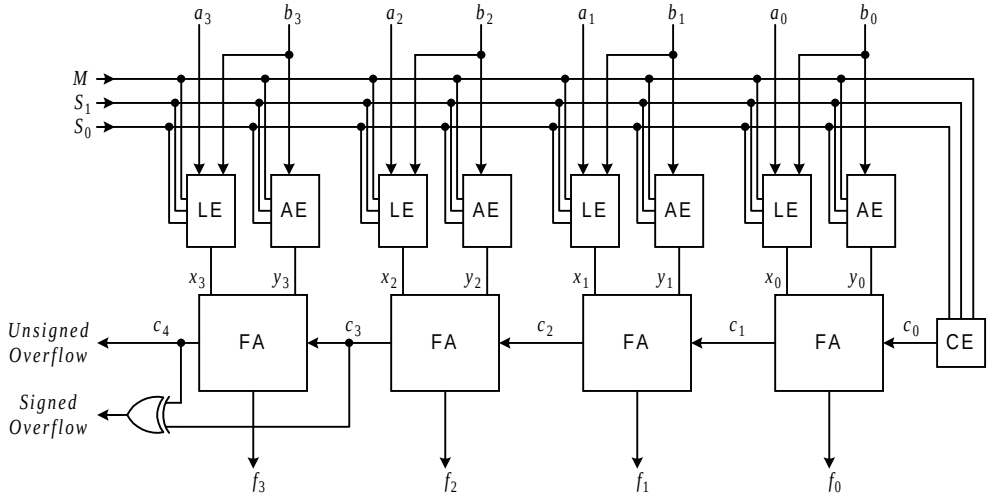
4. Design a 4-bit ALU that satisfies the following functional table:

M	S_1	S_0	Function
0	0	0	A AND B
0	0	1	A XOR B
0	1	0	All 0's, i.e. clear the output
0	1	1	Pass through operand A
1	0	0	Subtract $A - B$
1	0	1	Decrement A
1	1	0	not used
1	1	1	not used

The AE and LE circuits must be simplified. You need to draw the complete ALU circuit. (15)

Answer:

The overall general 4-bit ALU circuit is as follows:

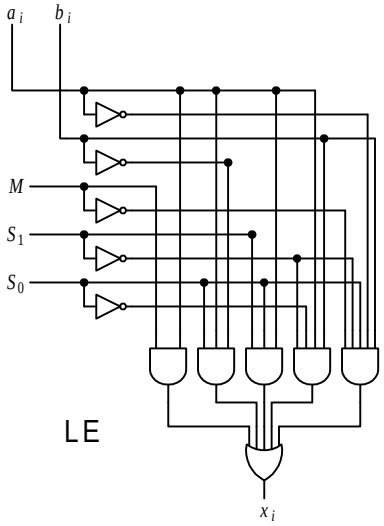


The truth table for the LE, AE, and CE according to the given functions is shown next:

M	S_1	S_0	Function	LE x_i	AE y_i	CE c_0
0	0	0	A AND B	$a_i b_i$	0	0
0	0	1	A XOR B	$a_i \oplus b_i$	0	0
0	1	0	All 0's, i.e. clear the output	0	0	0
0	1	1	Pass through operand A	a_i	0	0
1	0	0	Subtract $A - B$	a_i	b_i'	1
1	0	1	Decrement A	a_i	all 1's	0
1	1	0	not used	×	×	×
1	1	1	not used	×	×	×

The K-Map, equation and circuit for the LE is as follows:

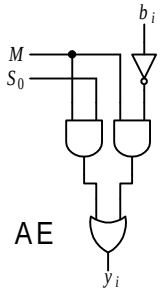
x_i : $a_i b_i$ / $S_1 S_0$	M = 0				M = 1			
	00	01	11	10	00	01	11	10
00	0	1	3 1	2	16	17	19 1	18 1
01	4	5 1	7	6 1	20	21	23 1	22 1
11	12	13	15 1	14 1	28 x	29 x	31 x	30 x
10	8	9	11	10	24 x	25 x	27 x	26 x



$x_i = Ma_i + S_0 a_i b_i' + S_1 S_0 a_i + S_1' S_0' a_i b_i + M' S_1' S_0 a_i' b_i$

The K-Map, equation and circuit for the AE is as follows:

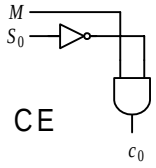
y_i : MS_1 / $S_0 b_i$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12 x	13 x	15 x	14 x
10	8 1	9	11 1	10 1



$y_i = MS_0 + Mb_i'$

The K-Map, equation and circuit for the CE is as follows:

c_0 : M / $S_1 S_0$	00	01	11	10
0	0	1	3	2
1	4 1	5	7 x	6 x



$c_0 = MS_0'$