CS/EE 120A

Homework #1 Given 1/18/01. Due 1/25/01

1. Any function can be implemented directly as specified or as its inverted form with a NOT gate added at the final output. Assume that the circuit size is proportional to only the number of AND gates and OR gates, i.e. ignore the number of NOT gates in determining the circuit size. Determine which form of the function (the inverted or un-inverted) will result in a smaller circuit size for the following function. Give your reason and specify how many AND and OR gates are needed to implement the smaller circuit.

$$F = x'y'z' + x'y'z + xy'z + xy'z' + xyz$$

2. Using AND, OR, and NOT gates, draw the circuit that implements the following function:

$$F(w, x, y, z) = \prod(0, 2, 6)$$

3. Convert the function $F = x'y'z + xy'z' + xy'z$ to:

   a) its standard form using the minimum number of logical operators.
   b) its nonstandard form using the minimum number of logical operators.

4. Perform the following calculations using 5-bit 2's complement binary arithmetic. Point out if there is an overflow error. Show your work.

a)
```
   01110
+  01010
```

b)
```
   01110
×  11010
```

c)
```
          _________
01101 )00100111
```