UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering
CS/EE120A – Logic Design
Homework 3
Given June 1, Due June 8, 2001

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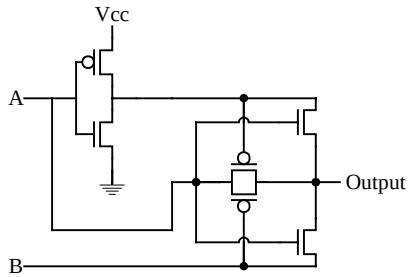
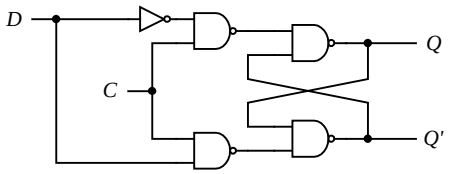
1. Determine the truth table for the following CMOS circuit (5)



Answer

A	*B*	*Output*
0	0	*Z*
0	1	*Z*
1	0	short circuit
1	1	short circuit

2. Determine the truth table for the following sequential circuit (5)



Answer

E	*D*	*Q*	Q_{next}	Q_{next}'
0	×	0	0	1
0	×	1	1	0
1	0	×	1	0
1	1	×	0	1