UNIVERSITY OF CALIFORNIA, RIVERSIDE

Department of Computer Science and Engineering
Department of Electrical Engineering
CS/EE120A – Logic Design
Final
Monday June 11, 2001, 11:30 – 2:30PM

32

Name: Solution Key **Student ID#:**
Please print legibly

Lab Section: 21 (TR 2-5):_____ **22** (MW 6-9):_____

(Numbers in parenthesis denote total possible points for question.)

1. Show using algebraic manipulation (axioms and theorems) that the following is true: (4)

$$x \odot (y \odot z) = x \oplus y \oplus z$$

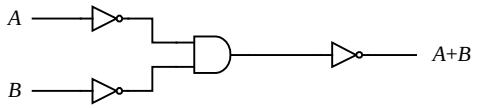
Answer

$$\begin{aligned} x \odot (y \odot z) &= (x \oplus (y \oplus z)')' \\ &= x(yz + y'z') + x' (yz + y'z')' \\ &= xyz + xy'z' + x' ((yz)' (y'z')') \\ &= xyz + xy'z' + x' (y' + z') (y + z) \\ &= xyz + xy'z' + \cancel{x'y'y} + x'y'z + x'yz' + \cancel{x'z'z} \\ &= xyz + x'y'z + xy'z' + x'yz' \\ &= (xy + x'y')z + (xy' + x'y)z' \\ &= (x \oplus y)' z + (x \oplus y)z' \\ &= x \oplus y \oplus z \end{aligned}$$

2. Implement by drawing the circuit of a 2-input OR gate using only AND and NOT gates. (4)

Answer

A+B = (A+B)′ ′ double prime
= (A′•B′)′ De Morgan's

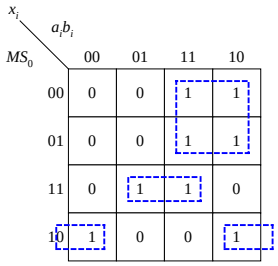


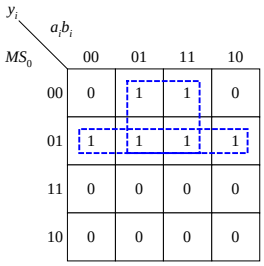
3. Design a 4-bit ALU with the following operations. You need to draw the full ALU circuit, AE, and LE. Optimize your AE and LE circuit with the least number of gates. (4)

M	S_0	Operation
0	0	A + B
0	1	A – 1
1	0	NOT B
1	1	Pass through B

Answer

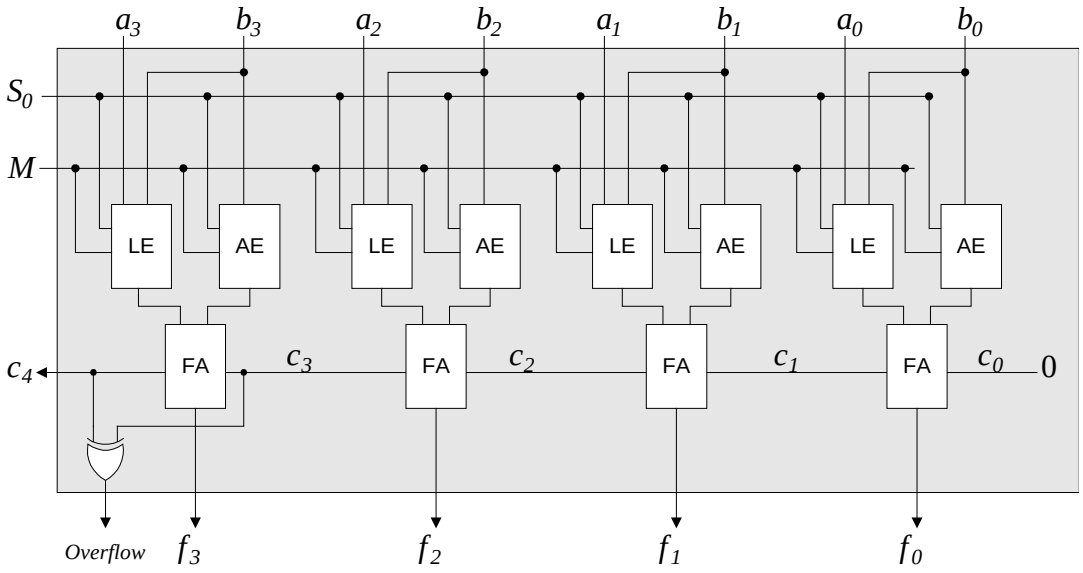
M	S_0	Operation	LE x_i	AE y_i	c_0
0	0	A + B	a_i	b_i	0
0	1	A – 1	a_i	1	0
1	0	NOT B	b_i'	0	0
1	1	Pass through B	b_i	0	0

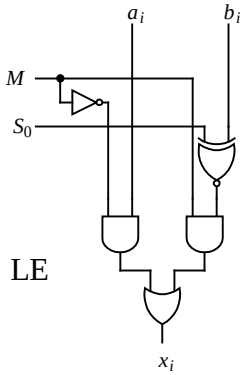


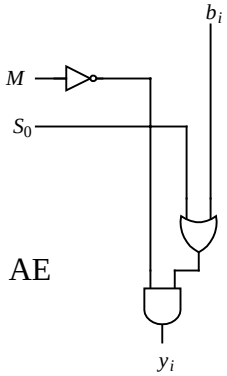


$x_i = M'a_i + MS_0b_i + MS_0'b_i'$
$= M'a_i + M(S_0 \odot b_i)$

$y_i = M'b_i + M'S_0$
$= M'(b_i + S_0)$





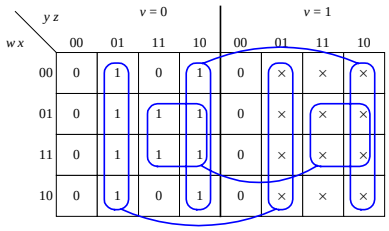


4. Use the K-map method to simplify a five variable (*v*, *w*, *x*, *y*, *z*) function with the following 1-minterms and don't care minterms: (4)

   - 1-minterms: v'w'x'y'z, v'w'xy'z, v'wx'y'z, v'wxy'z, v'w'xyz, v'wxyz, v'w'x'yz', v'w'xyz', v'wx'yz', v'wxyz'
   - don't care minterms: vw'x'y'z, vw'xy'z, vwx'y'z, vwxy'z, vw'x'yz', vw'xyz', vwx'yz', vwxyz', vw'x'yz, vw'xyz, vwx'yz, vwxyz

   Write the resulting simplified Boolean function.

Answer



$F = y'z + yz' + xy$

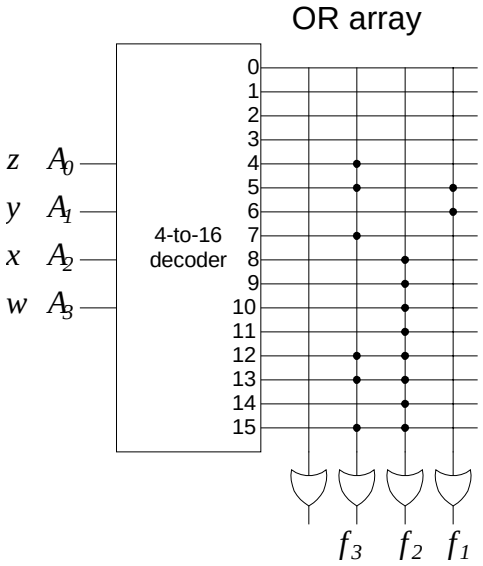
5. Use one 16 × 4 ROM (4 address lines, 16 entries, 4 data lines) to implement the following functions: (4)

$f_1 = w'xy'z + w'xz$

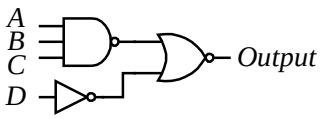
$f_2 = w$

$f_3 = xy' + xyz$

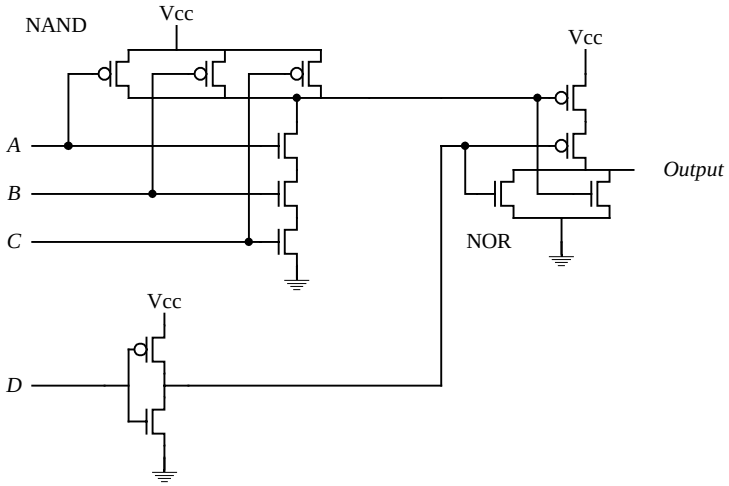
Answer



6. Implement the following gate level circuit using CMOS transistors. (4)



Answer



7. Given the following entity definition and operational table for an ALU, write the behavioral VHDL code for the corresponding architecture section of the ALU. (4)

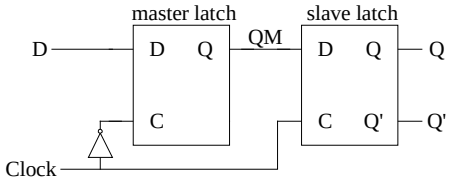
```
ENTITY alu IS
  PORT (M:   IN std_logic; -- select between arithmetic and logic operations
        S:   IN std_logic_vector(1 downto 0);   -- select for operations
        A, B: IN std_logic_vector(3 downto 0); -- input operands
        F:   OUT std_logic_vector(3 downto 0)); -- output
END alu;
```

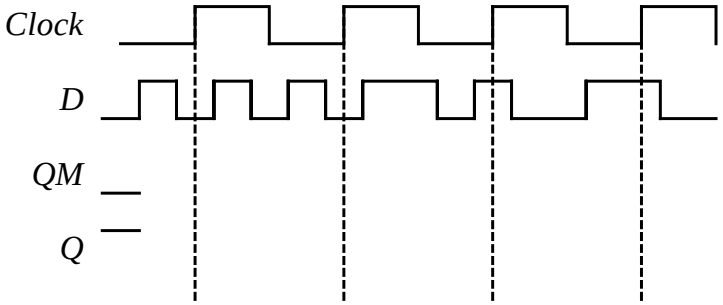
M	S_1	S_0	Operation
0	0	0	Add
0	0	1	Pass A through
0	1	0	Pass B through
0	1	1	Subtract
1	0	0	A AND B
1	0	1	A OR B
1	1	0	NOT B
1	1	1	Pass A through

Answer

```
ARCHITECTURE Behavior OF alu IS
BEGIN
  process(s, A, B)
  begin
    IF M = '0' THEN
      CASE s IS
      WHEN "00" =>
        F <= A + B;
      WHEN "01" =>
        F <= A;
      WHEN "10" =>
        F <= B;
      WHEN "11"
        F <= A - B;
      END CASE;
    ELSE                -- M = '1'
      CASE s IS
      WHEN "00" =>
        F <= A AND B;
      WHEN "01" =>
        F <= A OR B;
      WHEN "10" =>
        F <= NOT B;
      WHEN "11"
        F <= A;
      END CASE;
    END IF;
  end process;
END Behavior;
```

8. Given the following D flip-flop circuit, complete the trace for QM and Q in the timing diagram below: (4)





Answer

When *Clock* = 0, *QM* follows *D*. When *Clock* = 1, *Q* follows *QM*.