DEVASHREE TRIPATHY

http://www.cs.ucr.edu/~dtrip003/

EDUCATION

Sep 2015 – Present

University of California at Riverside, Riverside, CA
Ph.D. Student, Computer Science, GPA: 3.9/4
Supervised by Distinguished Prof. Laxmi N. Bhuyan

Council of Scientific and Industrial Research- Central Electronics Engineering Research Institute June 2014
(CSIR-CEERI), Pilani, India
M.Tech, Advanced Electronics Systems, GPA: 8.53/10
Thesis title: "Patient Assistance System using Brain Computer Interface"
Supervised by Prof. Jagdish Lal Raheja

Veer Surendra Sai University of Technology(formerly UCE), Burla, India May 2012
B.Tech, Electronics and Telecommunication Engineering, GPA: 9.69/10

SKILLS

Programming C/C++, CUDA, Verilog, VHDL, Assembly x86, Python, System C, HTML, MATLAB
Applications Saber, Mplab, LabView, Xilinx ISE, Quartus, Pspice, ModelSim, Synopsys Design Compiler, Altera
Others Linux, Windows, LaTeX, Microsoft Office

NOTABLE PROJECTS

Design of Memory Aware Warp Scheduler Apr – Oct 2017

- *Used* **C++** to modify GPGPU-Sim to implement efficient Warp Scheduling based on the feedback from Global memory, Caches and Register Files

Redesign of the GPGPU Execution Units to reduce Power Consumption through Efficient Warp-Scheduling Jan – Mar 2017

- *Used* **C++** to modify GPGPU-Sim to redesign the Execution units of GPU to **reduce the power consumption by 80%** and the compensate the performance loss by efficient Warp Scheduling

Wireframe: Supporting data-dependent parallelism through dependency graph execution in GPUs Jul – Nov 2016

- Used **C++** to modify GPGPU-Sim to manage dependencies among GPU thread blocks in order to **improve GPGPU performance by 45%**.

Latent Semantic Indexing using Non-Negative Matrix factorisation on GPU Sept – Nov 2016

- Used **CUDA** to implement the iterative updates of NMF factorisation
- Analysed the effectiveness of NMF for extracting latent semantic information from TREC documents Dataset w.r.t SVD.

Implementation of two-level round robin warp scheduling and dynamic warps on GPGPU-Sim Nov – Dec 2015

- Used **C++** to modify the source code of GPGPU-Sim, specifically its warp scheduling mechanism, for performance improvement.

*Patient Assistance System using Brain Computer Interface **(M.Tech Thesis)*** Jan – June 2014

- Used **MATLAB** to create the BCI Application to detect and quantify the features of the brain signals which indicated the user's intentions and translated these features into device commands to accomplish the user's intent. The project achieved a **classification accuracy of 96%.**

Optical Character Recognition using Neural Networks Sept – Dec 2013

- Processed the scanned images using feature extraction techniques.
- Customised neural network Algorithm was used to obtain an classification accuracy of 90% of the extracted characters.

An Improved Sobel Edge Detection Jan – Mar 2013

- Used **MATLAB** to improve the sobel edge detection of the Noisy images using Wavelet Transform.

Fingerprint Recognition using Gabor Filter Sept – Dec 2012

- Used **VHDL** to implement the Fingerprint image enhancement module and Gabor filter on Virtex II Pro FPGA.

Home Appliance Control using SMS Sept – Dec 2011

- SIM 300 GSM Modem used to send text message(SMS) and enable serial communication with microcontroller (ATMEGA 128).

COURSES TAKEN & MASTERED

Computer Architecture	GPU Architecture	Operating Systems
FPGA & Reconfigurable Systems	Data Mining	Compilers
High Performance Computing	Image Processing	Power Electronics
Data Mining	Real-time Embedded Systems	Algorithms

PUBLICATIONS

Abdolrashidi, A., Tripathy, D., Belviranli, M. E., Bhuyan, L. N., Wong, D., **"WIREFRAME: Supporting Data-dependent Parallelism through Dependency Graph Execution in GPUs**," 50th Annual International Symposium on Microarchitecture (MICRO 50), IEEE/ACM, 2017.
Patel, D., **Tripathy, D.**, Tripathy, C., **"*Survey of load balancing techniques for Grid,*"** Journal of Network and computer Applications, Vol- 65, pp: 103-119, Elsevier, 2016.

Patel, D., **Tripathy, D.**, Tripathy, C., **"*An Improved load-balancing mechanism based on deadline failure recovery for GridSim,*"** Engineering with Computers, Vol- 32(2), pp: 173-188, Springer, 2016.

Tripathy, L., **Tripathy, D.**, Tripathy, C., **"*Fault Tolerance in Interconnection Network-a Survey,*"** Research Journal of Applied Sciences, Engineering and Technology, Vol- 11(2), pp: 198-214, Maxwell Science Publishing, 2015.

Tripathy, D., Raheja, J., **"*Design and Implementation of brain Computer Interface Based Robot Motion Control,*"** FICTA, Springer, 2014.

Das, B., **Tripathy, D.**, Mishra, B., **"*The Crossed cube-Mesh: A New Fault-Tolerant Interconnection Network Topology for Parallel Systems,*"** International Journal of Emerging Technologies in Computational and Applied Sciences(IJETCAS), Vol- 7(1), pp: 211-219, 2014.

Pattanayak, D., **Tripathy, D.**, Tripathy, C., **"*Star-Mobius Cube: A New Interconnection Topology for Large Scale Parallel Processing,*"**International Journal of Emerging Technologies in Computational and Applied Sciences(IJETCAS), pp: 62-68, 2014.

ACADEMIC ACHIEVEMENTS

Awards & Achievements:

Qualified National-level science Talent Search Examination (NTSE) by United Council, India	2001
Qualified Mathematics Olympiad	2002
Top 0.1% among all the students at National level, Central Board of Secondary Education	2006
1st rank among all girls in freshmen year of VSSUT,Burla	2008
1st rank among all B.Tech students of VSSUT,Burla	2012
Quick-Hire Fellowship by Government of India	2012-2014
Dean's Distinguished Fellowship, UCR	2015

Languages | English (Fluent), Hindi (Native), Odiya (Native)