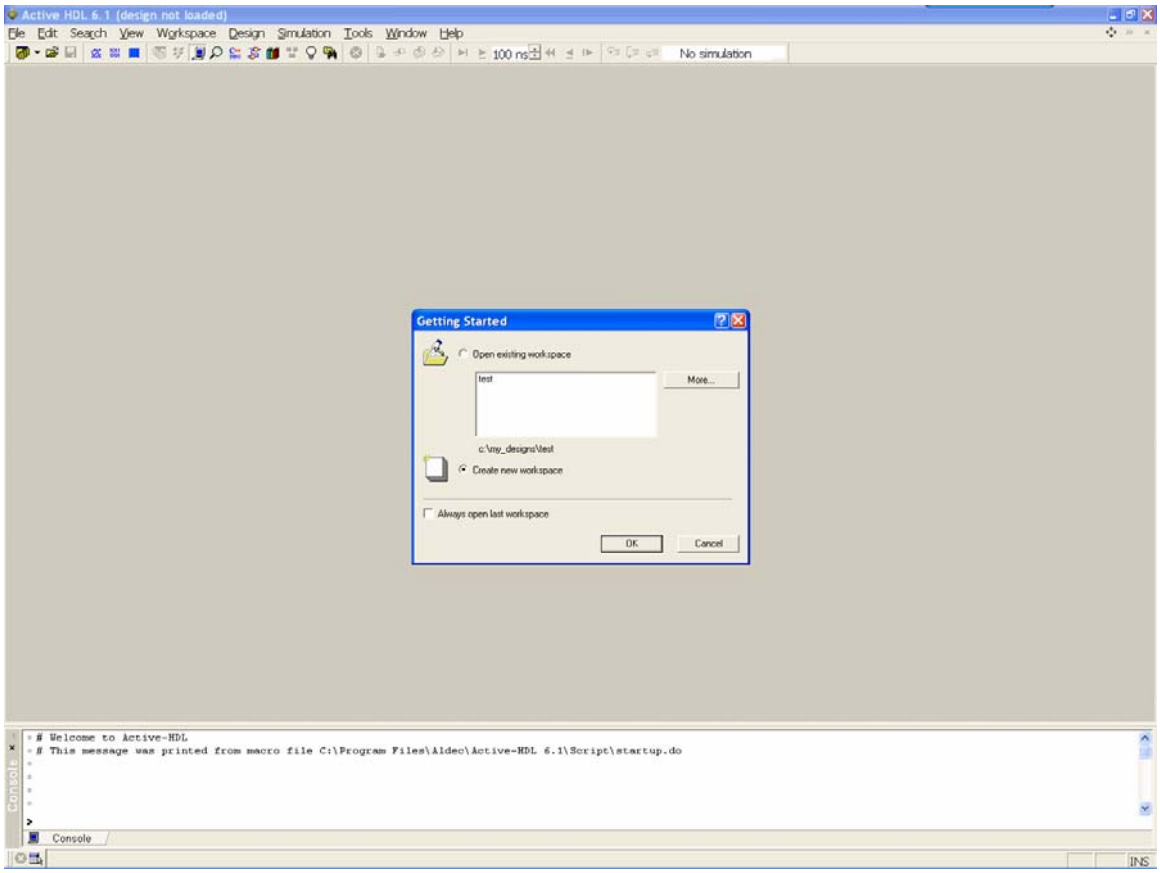
Active-HDL Manual

Content

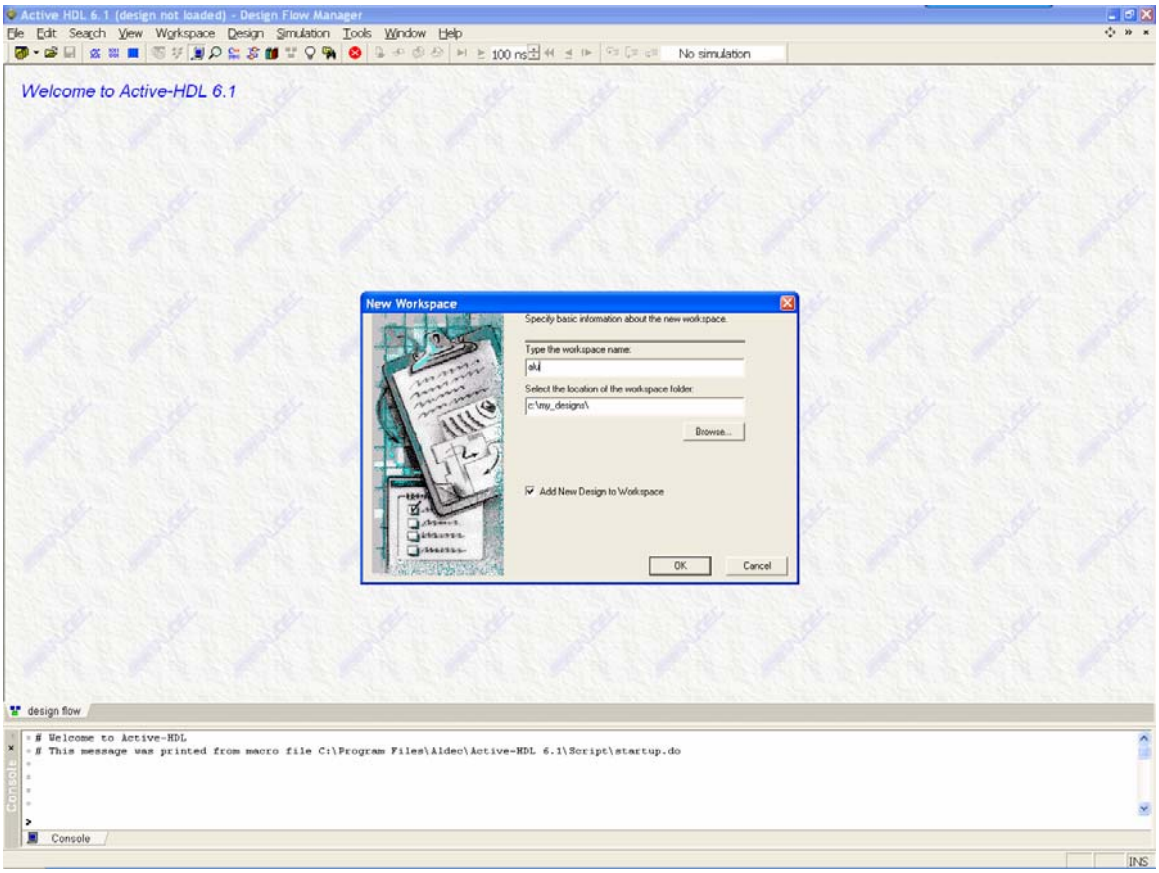
1. Create a design file (.vhdl)

1.1 Set up the programming environment

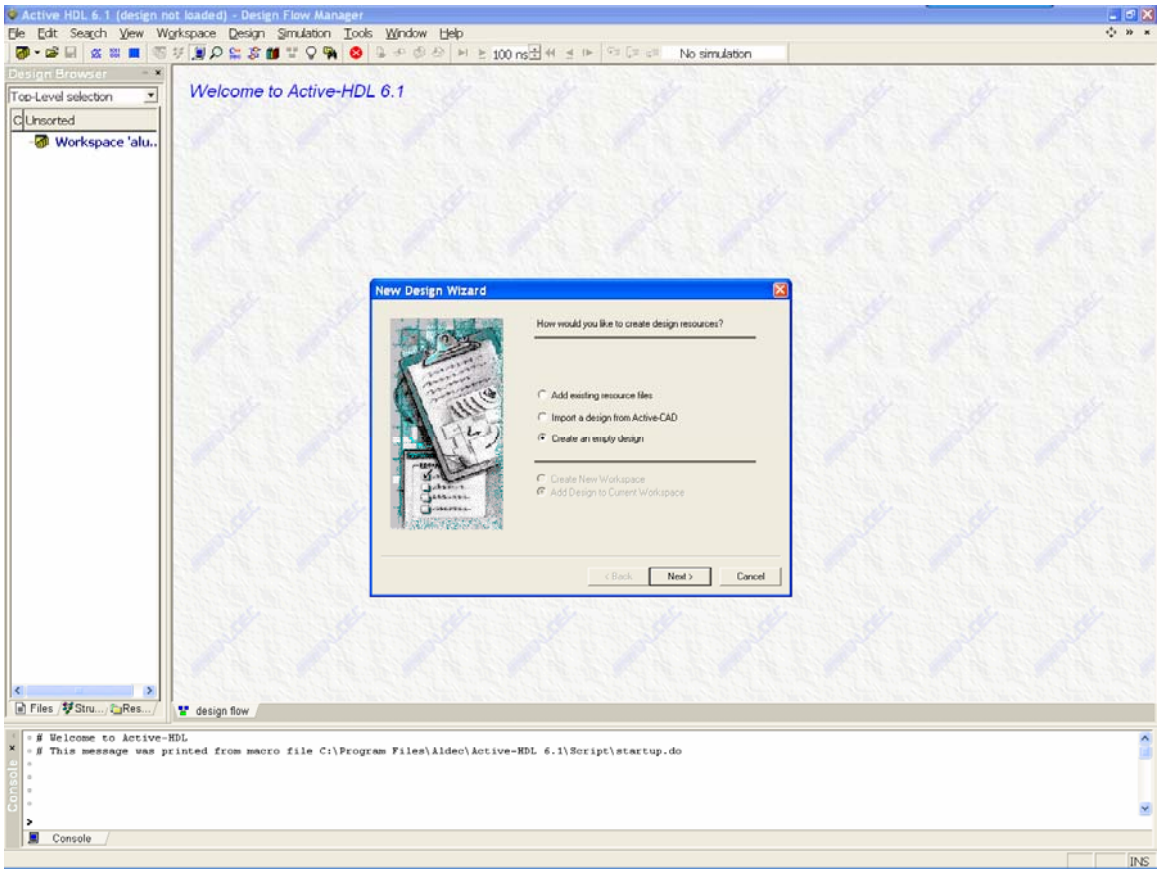
Step 1: Select “Create new workspace”



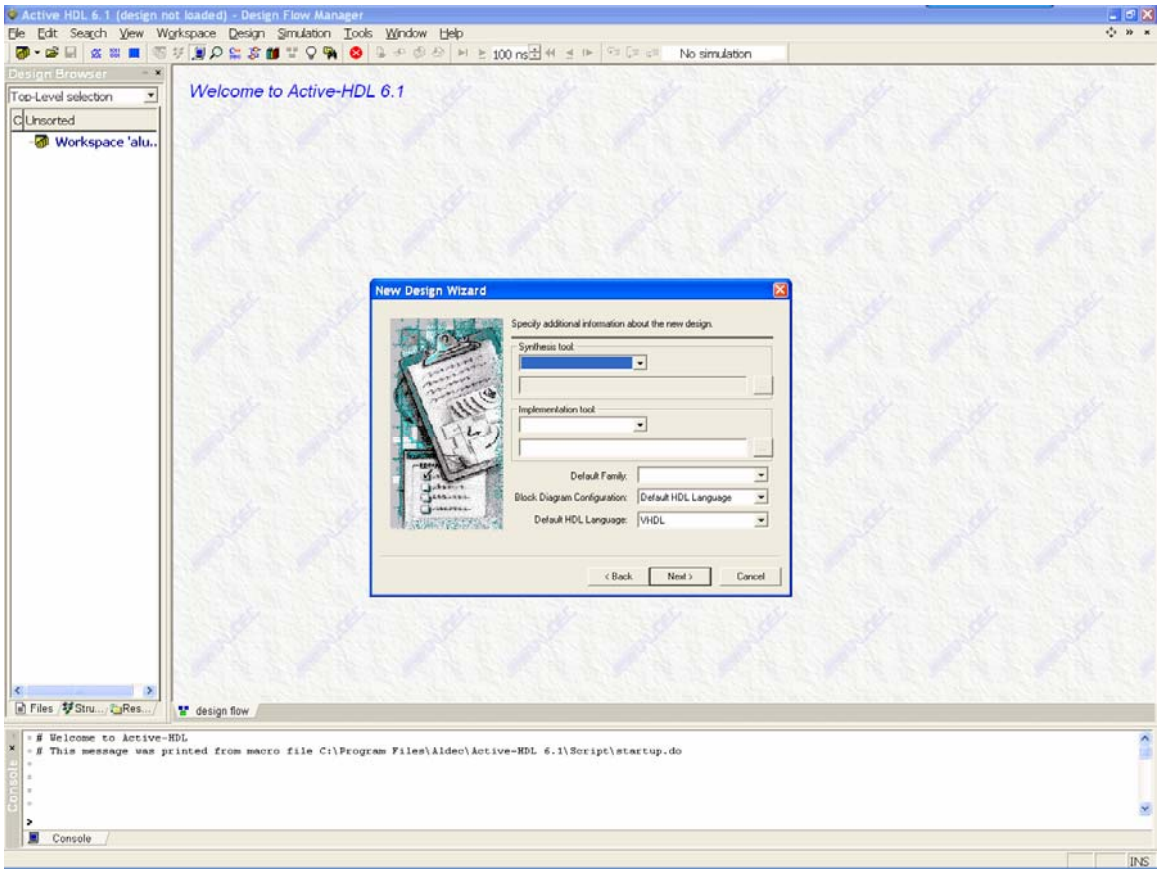
Step 2: Type in the workspace name and choose a proper directory (you may use the default one).



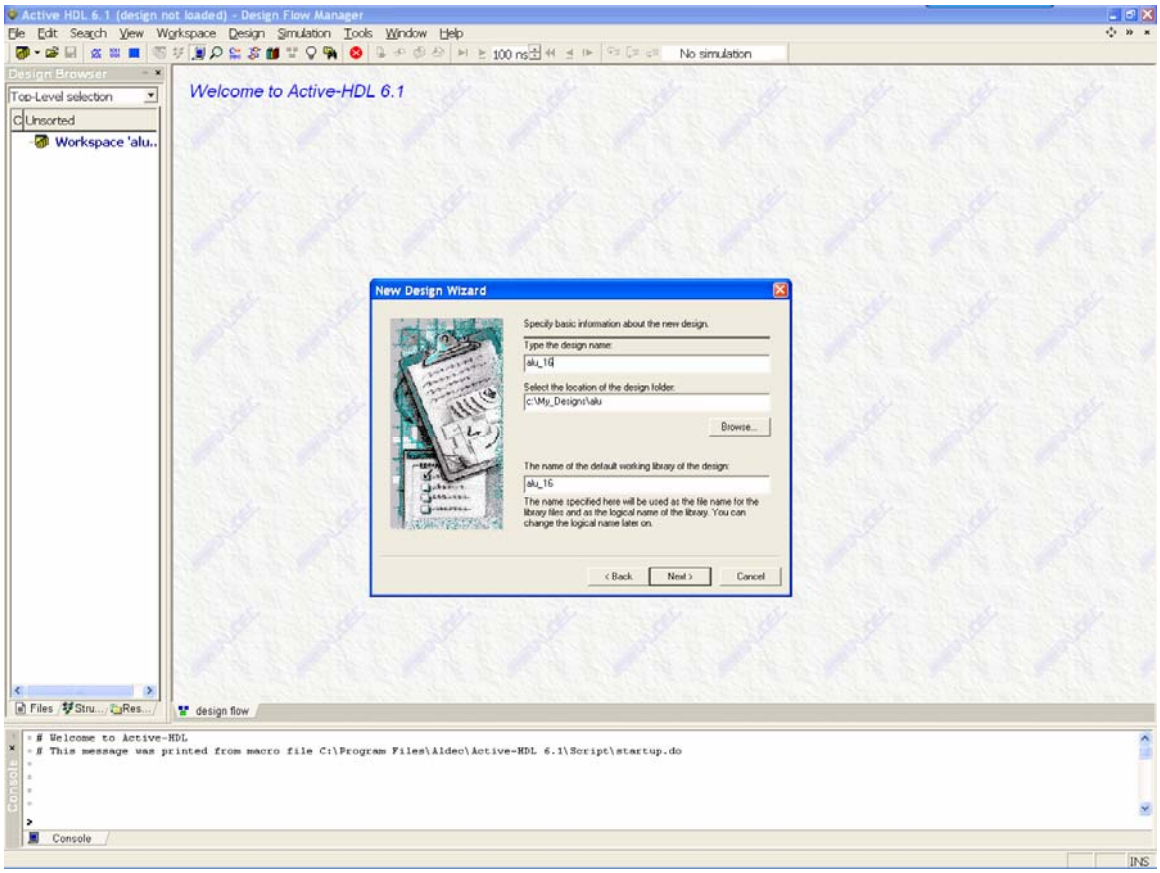
Step 3: Select “Create an empty design”. Next time you run Active-HDL, you may choose “Add existing resource files”



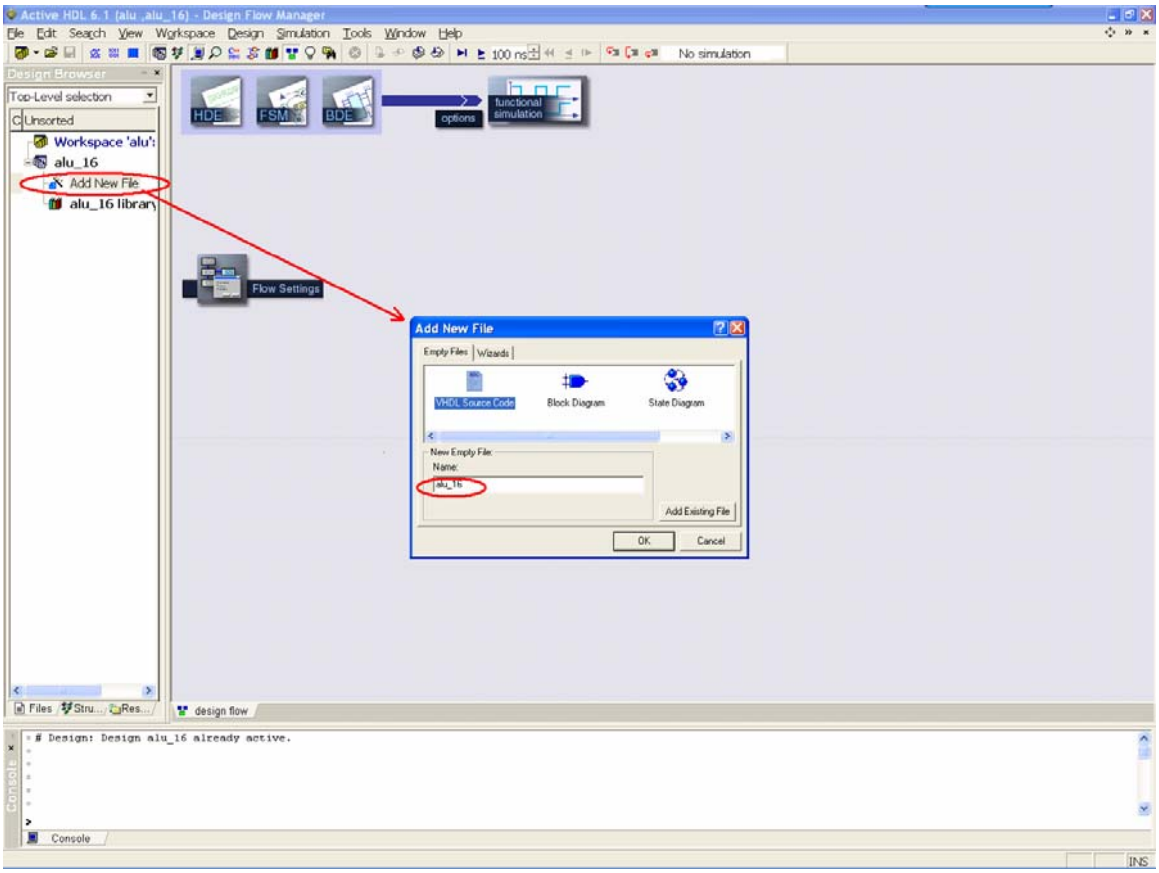
Step 4: Leave everything as it is, and click on next



Step 5: Type in the design name. Then click on “finish” to confirm.



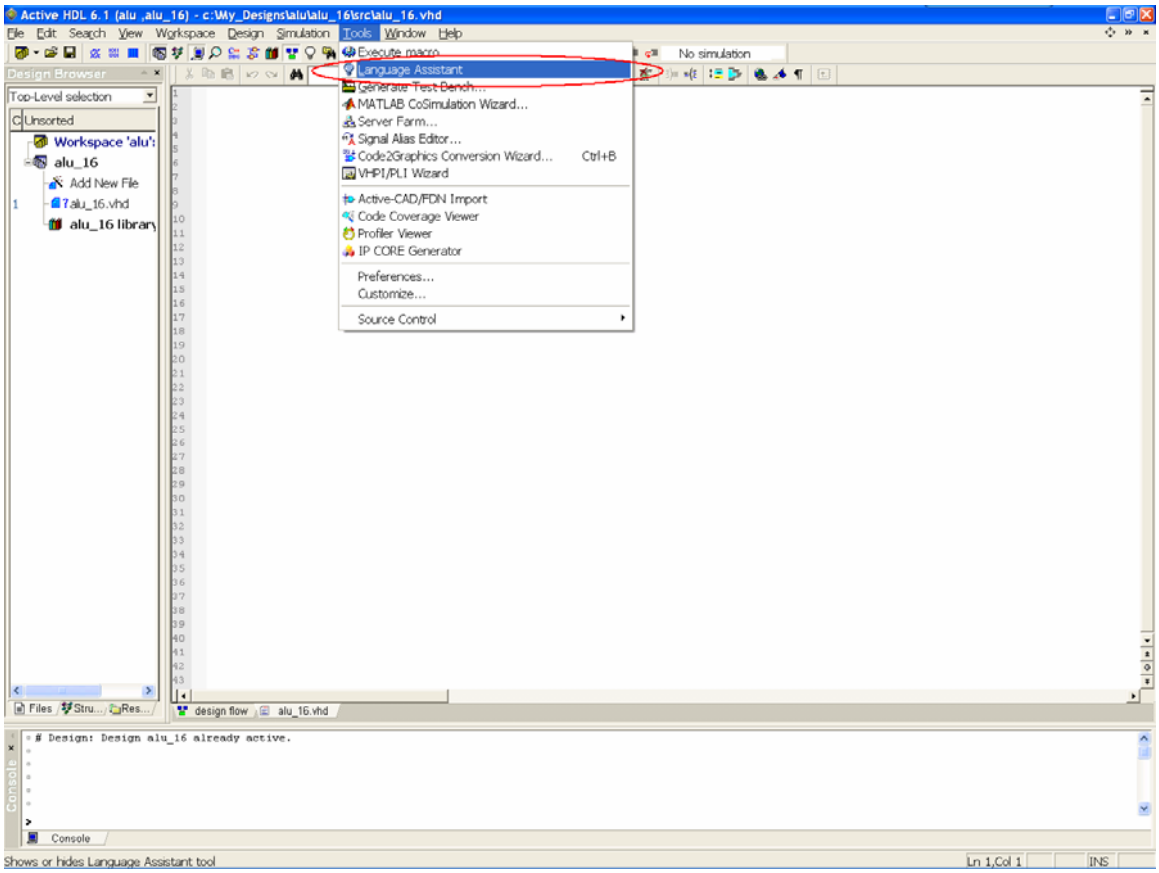
Step 6: Double click on "Add new file" on the design window to make the VHDL file.



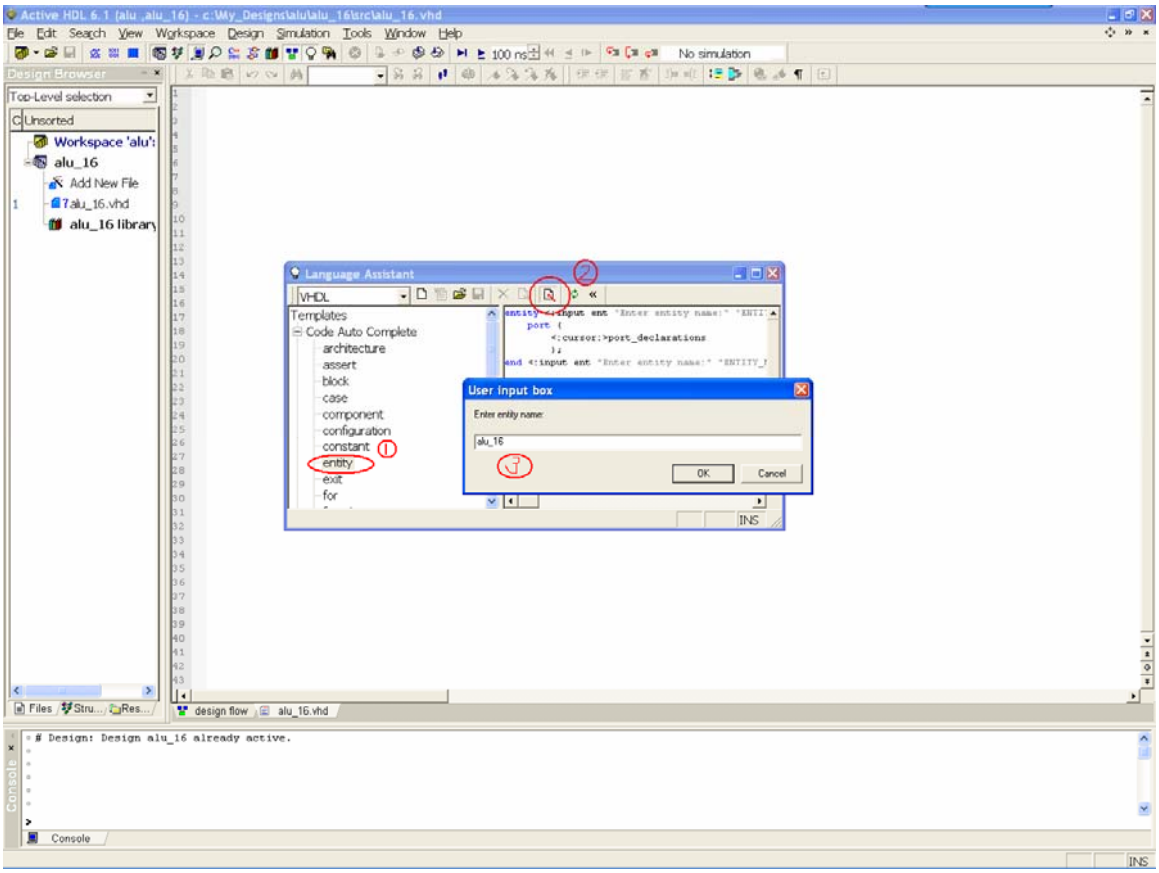
So far, we have finished everything we need before starting the design.

1.2 Create the design with Language Assistant (entity, architecture)

Step 1: Select “Language Assistant” from “Tools”

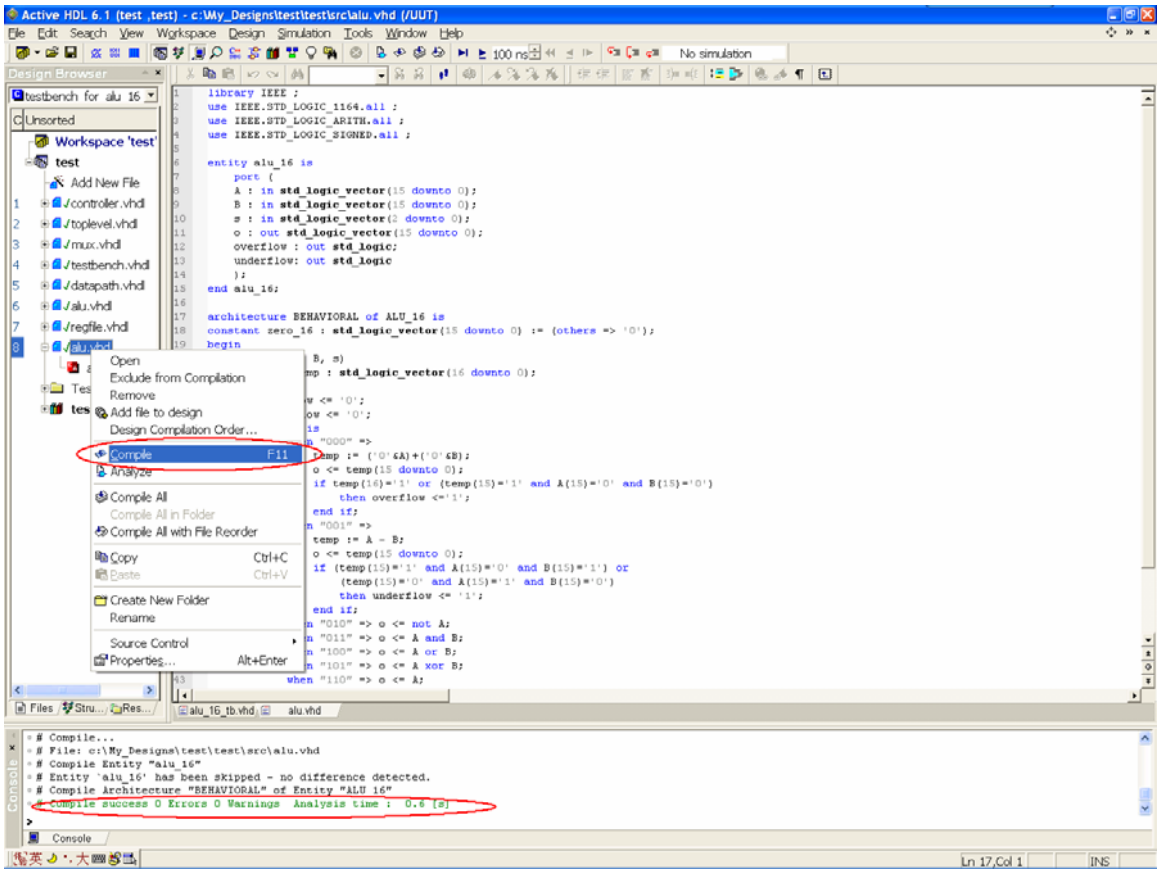


Step 2: Create Entities and Architectures. Just follow the information from the pop up window.



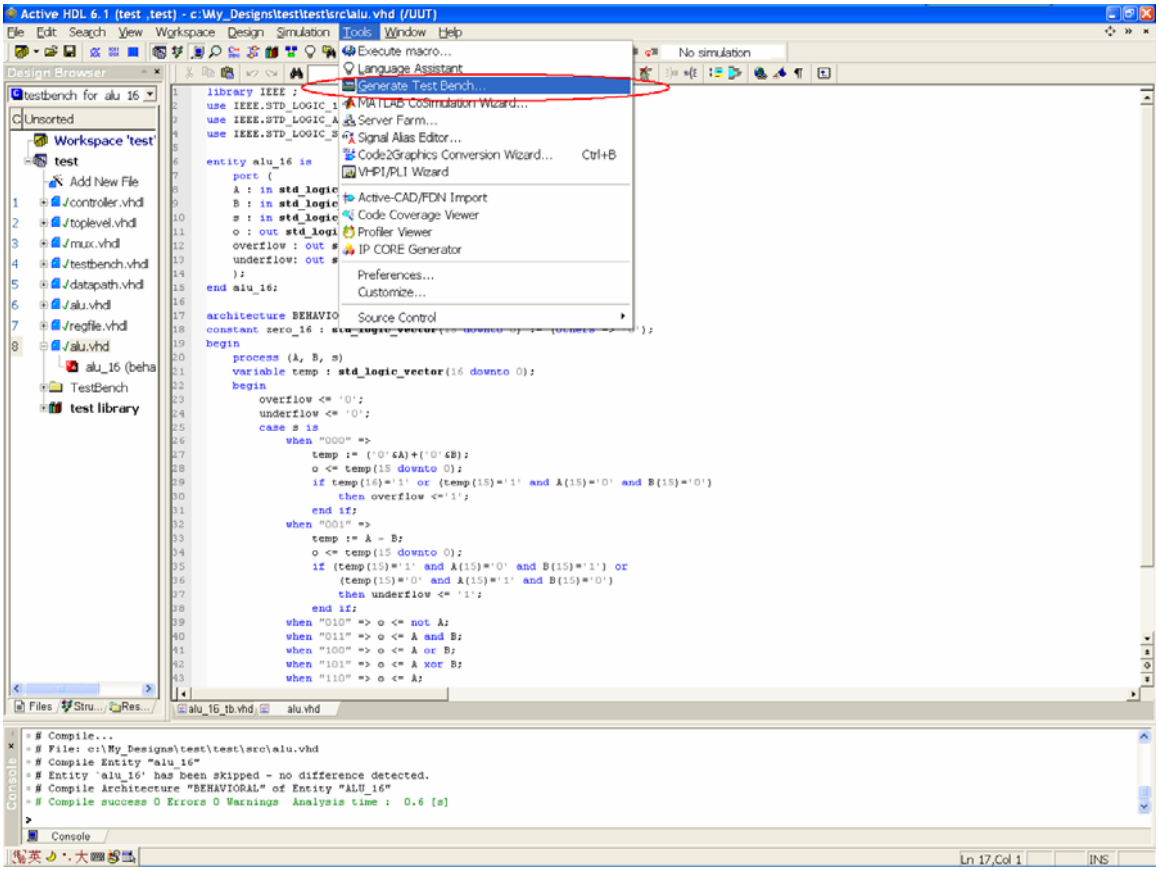
1.3 Compile (F11)

Once you have done with all the coding, you may start to compile. Click on F11 or right-click on the file name appearing on the design window. If an error is confronted during the compilation, a red line will be shown underneath the problematic line in the source code. Otherwise, you will find **GREEN** success information in the command window at the bottom of the page.


Active HDL 6.1 (test ,test) - c:\My_Designs\test\test\src\alu.vhd (/UUT)
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
testbench for alu 16
Unsorted
Workspace 'test'
test
Add New File
controller.vhdl
toplevel.vhdl
mux.vhdl
testbench.vhdl
datapath.vhdl
alu.vhdl
regfile.vhdl
alu_vhd
Open
Exclude from Compilation
Remove
Add file to design
Design Compilation Order...
Compile F11
Analyze
Compile All
Compile All in Folder
Compile All with File Reorder
Copy Ctrl+C
Paste Ctrl+V
Create New Folder
Rename
Source Control
Properties... Alt+Enter
library IEEE ;
use IEEE.STD_LOGIC_1164.all ;
use IEEE.STD_LOGIC_ARITH.all ;
use IEEE.STD_LOGIC_SIGNED.all ;
entity alu_16 is
port (
A : in std_logic_vector(15 downto 0);
B : in std_logic_vector(15 downto 0);
s : in std_logic_vector(2 downto 0);
o : out std_logic_vector(15 downto 0);
overflow : out std_logic;
underflow: out std_logic
);
end alu_16;
architecture BEHAVIORAL of ALU_16 is
constant zero_16 : std_logic_vector(15 downto 0) := (others => '0');
begin
alu_16_tb.vhd
alu.vhd
Compile...
File: c:\My_Designs\test\test\src\alu.vhd
Compile Entity "alu_16"
Entity 'alu_16' has been skipped - no difference detected.
Compile Architecture "BEHAVIORAL" of Entity "ALU_16"
Compile success 0 Errors 0 Warnings Analysis time : 0.0 [s]
Console
Ln 17,Col 1
INS

2 Create a benchmark

2.1 Use Generate Test Bench from the Tool bar. Just follow the instructions. (You may simply use all the default settings.)



2.2 Create benchmark with Language Assistant (process statement, assert)

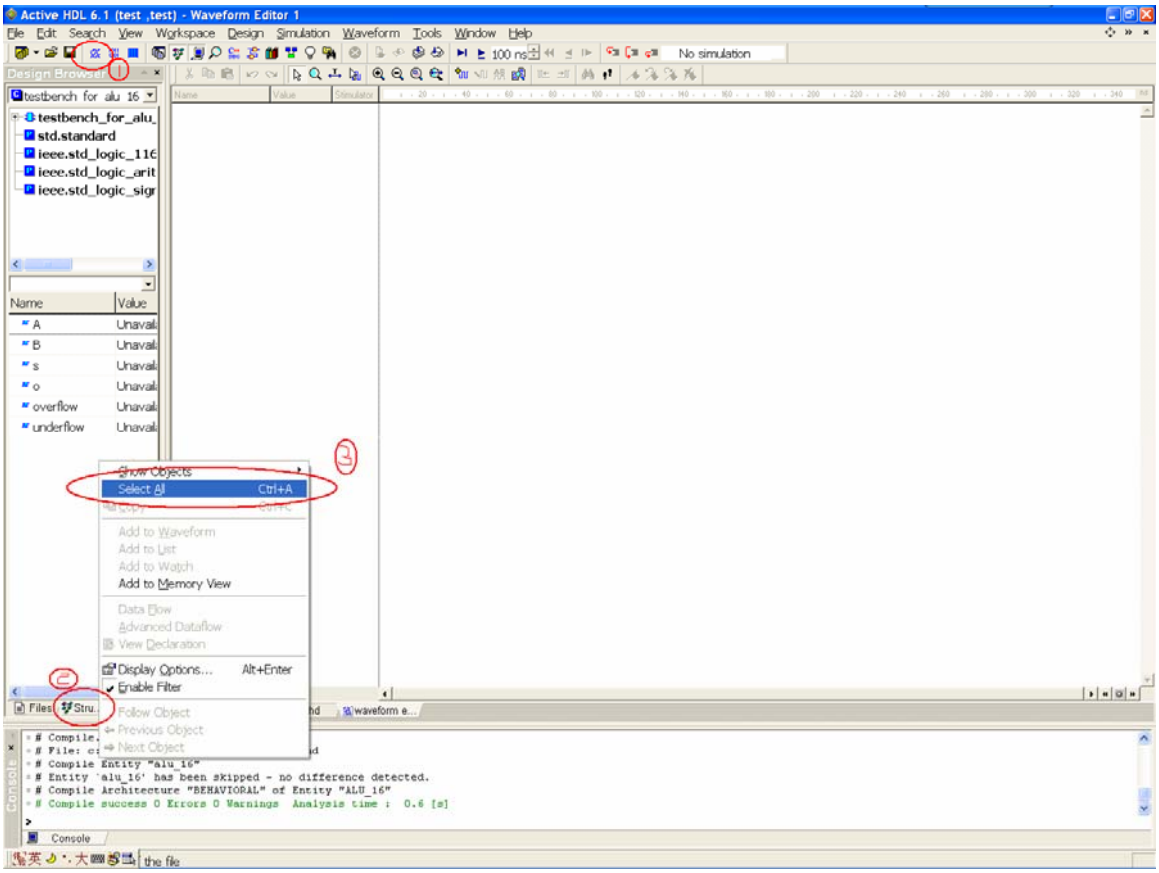
2.3 Compile (F11)

Step b and c are the same as what we did when create a design file. Use that part as reference. After this step, we will have a test bench for our original file. Later on, we are going to verify the code with wave forms. See if the test bench runs correctly with our code.

3 Create a new Waveform

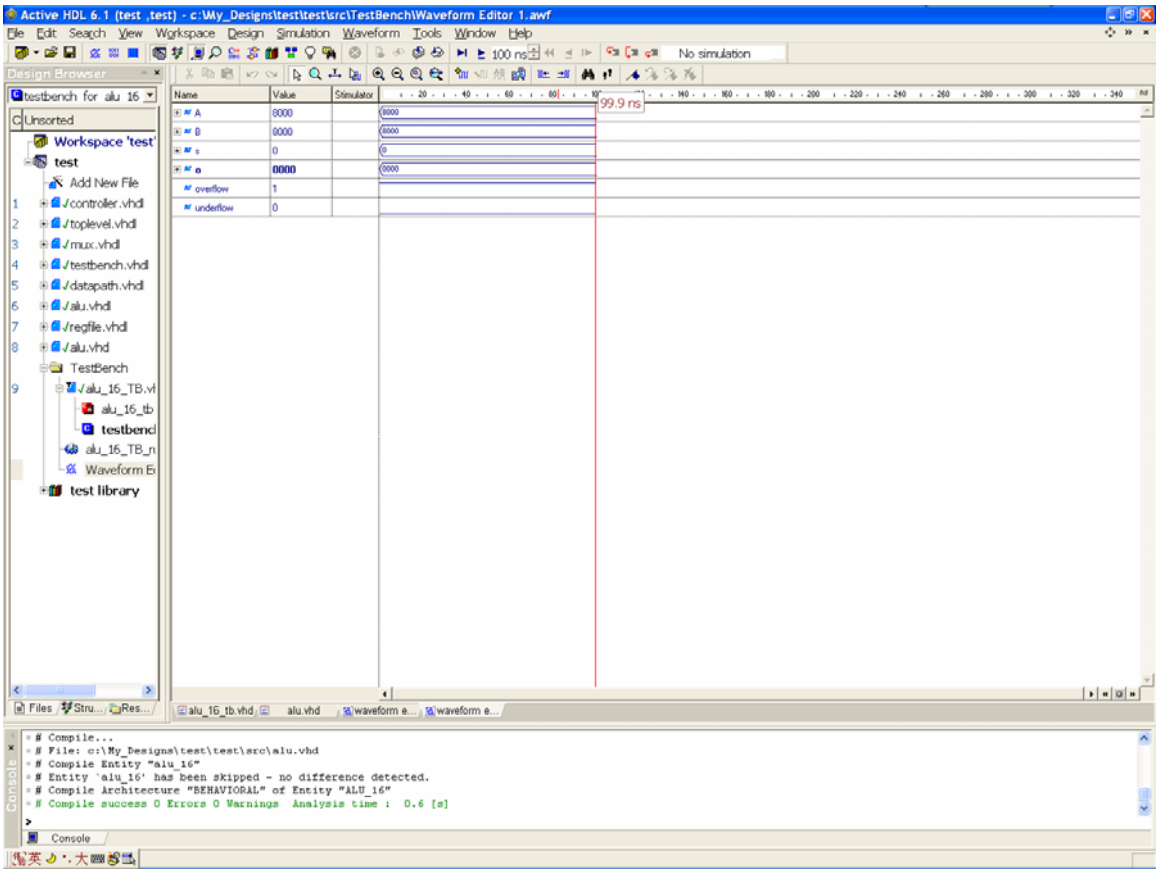
3.1 set up for a wave form

Click on “New WaveForm” from the tool bar. Then select “Structure” sheet at the bottom of the Design Browser to change a different view, in which we will find all the signals. After that, click on the test bench name, and select all the variables (input and output) and drag them to the wave form window



3.2 Run the simulation

Click on F5 to start the simulation. Check all the wave forms for the cases you've listed in the test bench. Modify the design file if there is something wrong.


Active HDL 6.1 (test ,test) - c:\My_Designs\test\test\src\TestBench\Waveform Editor 1.awf
File Edit Search View Workspace Design Simulation Waveform Tools Window Help
No simulation
Design Browser
testbench for alu_16
Unsorted
Workspace 'test'
test
Add New File
controller.vhd
toplevel.vhd
mux.vhd
testbench.vhd
datapath.vhd
alu.vhd
regfile.vhd
alu.vhd
TestBench
test library
Name
Value
Stimulator
A
B
s
o
overflow
underflow
99.9 ns
Compile...
File: c:\My_Designs\test\test\src\alu.vhd
Compile Entity "alu_16"
Entity 'alu_16' has been skipped - no difference detected.
Compile Architecture "BEHAVIORAL" of Entity "ALU_16"
Compile success 0 Errors 0 Warnings Analysis time : 0.6 [s]
Console