Acquisition of an Ultra Low-Latency Multiprocessor System with On-Board Hardware Accelerators

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Project Summary

The University of California at Riverside has active research programs in Computer Science and Engineering, mostly supported by NSF, which require extensive computational and networking capabilities. To facilitate and enhance them, this proposal requests the acquisition of a Cray XD1 cluster with a total of 96 2.4 GHz Opteron CPUs.

Intellectual merit: We will develop efficient scalable algorithms and software resource management schemes for individual applications. We contemplate using the proposed Cray XD1 cluster in support of six projects at the outset: (1) investigation into scalable hardware and software design for Internet web servers and data centers; (2) symbolic model checking; (3) pattern discovery for a variety of biological applications; (4) automatic compilation of high-level code, such as C or FORTRAN, into RTL VHDL code; (5) warp processing; and (6) augmenting existing microarchitecture with security protections to ensure the integrity and confidentiality of program execution. All these projects will greatly benefit from the availability of the XD1 cluster, which is particularly suitable because (1) it can be partitioned into four different sub-clusters that can work independently and simultaneously on different applications, (2) it provides ultra low message passing latency within a sub-cluster and between sub-clusters, and (3) it provides an SMP environment with four processors that can be used for tightly-coupled codes, thus a hybrid programming model suitable for different applications.

Another innovative characteristic of the Cray XD1 is that it provides FPGAs that can be used as customizable hardware accelerators for applications with highly-localized computation-intensive loops. Unlike other FPGA-based systems, the Cray XD1 FPGAs are connected to the system bus and have direct access to the shared memory. In addition to the application projects, which can benefit from a hardware accelerator, our research projects on FPGA compilation, hardware/software partitioning, and CPU micro architecture design need an FPGA-based system for a test bed.

Broader impact: Besides producing research results, the cluster will be used in various graduate courses at UCR, stimulate interdisciplinary research, and precipitate new collaborations in multiple areas of science and engineering. The cluster will be a computational resource made available to other departments at UCR through a high-bandwidth fiber-optic connection. As UCR is a Minority Institution and the most diverse campus of the UC system, this cluster will play a role in our outreach efforts to the community (which is predominantly made up of underrepresented minorities) and prospective students. As UCR continues to grow, the cluster also will enable us to attract highly-sought-after professors, thus enabling us to increase the diversity of our faculty.