

## **ABSTRACT**

### **Scheduling in High-Performance Internet Routers**

As Internet expands, the demand on routers for more bandwidth and better quality of service (QoS) increases exponentially. Current routers employ input-queued crossbar switches that require sophisticated scheduling techniques for packet transmission. In this project, new packet-based scheduling algorithms are developed and tested for high-performance Internet router operation. Fair scheduling algorithms are also incorporated in the crossbar to allocate bandwidths proportional to the request reservations of the packets. Both flow-based and port-based fair scheduling algorithms are designed similar to the deficit round-robin technique. To scale these routers to terabit bandwidth, architectures for fully connected crossbar switches and router topologies are also developed based on scalable networks. Scheduling and routing algorithms for these networks are investigated.

The intrinsic merit of the proposed research lies in the development of new scheduling techniques for different switch organizations of an IP router that perform optimally for the Internet traffic. The algorithms are tested both through network simulation and hardware experiments. A trace-driven configurable simulation test-bed is developed, where publicly available Internet traces can be fed as the input workload. The crossbar switch and scheduling algorithms are implemented in hardware using field programmable gate arrays (FPGAs) and SRAMs. Such an implementation produces an accurate analysis of the proposed algorithms and their hardware complexities. The broader impact of the work is evident through quality publication, industrial collaboration, and student education funded through this project.