CS 213 Parallel and Distributed Processing
Test 1, 30 points

1. (a) What is Amdahl's law for parallel processing? What are its limitations? 2 pts.
(b) State the main difference between SIMD vs. MIMD, shared memory vs. message passing, and centralized memory vs. distributed memory computers. 3 pts.
(c) Using the above terms, describe a category for the following commercial machines: Sequent Balance, IBM SP-2, Cray T3D, CM-5, Maspar and SGI Origin. 3 pts.

2. (a) Draw the topologies of a ring, a 2-D torus and a hypercube network, and give expressions for their diameter for a network of size N. 3 pts.
(b) Assume a link bandwidth of 10 Mbits/sec, sending overhead of 230 microsecs and receiving overhead of 270 microsecs. The packet length is 1000 bytes. Assume that the flight time between any two nodes and header processing time at a node are negligible. Derive the worst-case delays in the above three networks of size 16 for packet switching and wormhole routing. 5 pts.

3. (a) Draw an 8x8 Omega network using 2x2 switches and show the connection between input 3 (011) and output 5 (101) in bold. Explain how a packet is routed from source S to destination D. 3 pts
(b) Determine the number of stages and number of switches required to connect N inputs to N (N=k**n) outputs using kxk switches? Assuming the hardware complexity of a kxk crossbar switch to be k**2, what is the cost optimal design of a 16x16 network? 4 pts.

4. (a) Draw a state diagram for the Write Once protocol. Explain a how a block moves to the reserved state. What are the conditions for a block to exit from the reserved state to Valid, Invalid and Dirty states? 4 pts.
(b) What is false sharing? Assume that words x1 and x2 are in the same cache block in a clean (valid or shared) state in the caches of P1 and P2. Assuming the following sequence of events, identify each case as a true miss or false sharing miss or a hit. Explain your answer.

Time	P1	P2
1	write x1	
2		read x2
3	write x1	
4		read x1

3 pts.