Poster Abstract: Splitting The Sensor Node

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ABSTRACT
The current trend of computationally intensive applications such as audio capture, FFT, image sensing, motion detection, feature extraction and cepstrum calculations being ported to the sensor domain, alludes towards the need to handle copious amounts of data in comparison to rudimentary temperature and humidity sensing applications. Developing a split architecture based sensor platform is an effective and efficient methodology to reach the crucial goal of *in-situ* processing of data. Resulting in a direct reduction in the amount of information needed to be transmitted over the wireless links. The Split-Node-Architecture (SNA) which we develop addresses this very crucial aspect of sensor network design. The suitability of employing the SNA architecture is demonstrated by its performance metrics obtained by running a 128point FFT benchmark. The higher throughput, of the SNA architecture enables faster data processing upto **24** times that of the Atmel AVR architecture (MICA). Additionally a **29%** improvement in power efficiency vis a vis popular sensor platforms, tilts the scales unambiguously in favor of the SNA. The low power consumption of the Co-S module, a part of SNA, results in savings upto **6uJ** per 128 point FFT operation when compared to the Stargate (Intel PXA 255).

Categories and Subject Descriptors
C. 4 [**Performance of Systems**]: Design studies, Performance attributes.

General Terms
Measurement, Performance, Design, Experimentation.

Keywords
Sensors, Split-architecture, performance, high capacity storage.

1. INTRODUCTION
Sensor platforms designed to live up to the expectations of the deployment specifications need not only to be power efficient [2] but also must incorporate the ability to reduce the amount of information passed via wireless links over the network in order to avoid depleting the complete setup of precious battery resources. The emerging class of applications aimed at this domain strive to conjure diverse autonomous [1] systems handling intrusion detection, voice based reporting systems, ecological monitoring [3], and many more. Applications such as these demand an ever greater level of processing capability from sensor nodes which are deployed in the field. Cepstrum calculation for resonance analysis [3], FFT, harmonic filtering and extraction, image masking and processing all require a significant level of processing capability to be demonstrated by the *Micro Controller Unit (MCU)* on the small power efficient nodes. Current implementations of such platforms, mostly utilize 8-bit MCU's which are unsuitable for the job. They simply do not possess enough processing capability to satisfy the compute intensive applications which are now being hived onto this domain. Our SNA architecture provides an avenue to merge the two most critical needs of the hour: increased computational capabilities and power frugal design. Through extensive experimentation and benchmarking we have designed the SNA based on the Co-S architecture integrated with the HP, a result of the ongoing RISE (RIverside Sensors) [3] project aiming for higher performance from sensor platforms which simultaneously satisfies the constraints of low power consumption, high capacity onboard storage and a small form factor. The SNA comprises of a dual processor split-level design and boasts of gigabyte scale onboard memory, courtesy of a power efficient SD-card. Sufficient for practically any deployable application in the sensor domain today. The SNA, based on a Co-Processing (Co-S) RENESAS M16C/28, 16 bit processor module integrated with a System on Chip (SoC) CHIPCON 1010 based (optimized 8051 core) Host Platform (HP) boasts a gigabyte scale energy efficient data storage system, simultaneously satisfying the constraints of low power consumption and small form factor. Our novel architecture not only allows us to implement a new "Sense and Store" (SoSt) paradigm, in clear contrast to the prevalent "Sense and Send" but also allows for *failover support* on the sensor platform, unheard of in the current sensors available for commercial and research purposes today. The SoSt paradigm, made possible by the SNA, due to its humongous onboard memory storage capacity pivots on logging sensed events unless absolutely necessary to transmit. It is in this regard that we exploit advances in low power, ultra high capacity non-volatile storage devices, thus paving the way for integration of widely available, cheap and power efficient flash memory storage devices, namely the SD-Cards, Compact Flash, XD-Cards. The SNA based RISE platforms were motivated by the requirements of the Bio-Complexity and the James Reserve Projects at the Center of Conservation Biology (CCB) at UC Riverside, working towards

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the conservation and restoration of species and ecosystems by collecting and evaluating scientific information.

2. SNA Architecture

2.1 Processing Architecture

The design policy for the SNA, consistently has been to reduce power consumption, maintain software compatibility vis-à-vis TinyOS and simultaneously broaden the spectrum of applications of compact sensor systems. In keeping with our goals, the HP employs a monolithic SoC device which sports a power optimized 8051 core, radio, 3 ADCs, 2KB SRAM, 32 KB on-chip-flash, 2 UARTs, SPI bus, all onto a single SoC architecture and an interface layer with the Co-S, completes the SNA. On one hand this simplifies hardware design due to integration of all the components onto a single chip, while on the other hand overall system power consumption is reduced due to tightly integrated peripherals on the chip. Our architecture differs from existing platforms not only in terms of its computing power, flexibility, level of on-chip component integration but also, and quite significantly in the amount of on-board storage memory that it can provide, and an added software paradigm of SoSt which manages extremely large amounts of raw data from the sensing hardware in-situ, before transmitting relevant parts of it efficiently to the base station. A quick calculation of the power consumption of our platform reveals orders of enhancement in power efficiency, which is obtained when a gigabyte capacity SD Card is integrated with the sensor platform instead of EEPROMs (MICA). Assuming, 100KB worth of data needs to be gathered by the sensor during a particular time interval, a realistic figure for temperature and CO_2 sensors. In order to store the data on the SD card, we measured, in real-time, the overall energy consumed to be a miniscule 245.6mJ, while storing the same amount of data on the EEPROM available on the MICA would entail consumption of 2450mJ [2], and transmitting it via the wireless interface, assuming no errors, consumes 16,473mJ. The major contributing factor towards the lower energy consumption of the SDCard is the faster data transfer rate on the SPI Bus (80KB/s), with respect to the EEPROM (1.6KB/s), or the wireless transmitter (1.92KB/s). This simple experiment highlights the advantages of utilizing better storage solutions along with intelligent data management techniques which is one of the compelling motivations discussed in this poster, vis-à-vis the design of sensor architectures that can handle copious amounts of data, store and process them for mining intelligent patterns within. Therefore, newer generation of sensors, can thus afford the luxury of storing vast amounts of data, (Gigabyte scale), on board, and in employing these devices lies the crux of the SoSt paradigm. We exploit the Renesas M16C/28, based Co-S platform by offloading onto it computationally intensive task of frequency domain analysis, i.e. calculation of Fast Fourier Transform (FFT). This endows the SNA with a dual pronged advantage, the first being, higher throughput along with low power consumption, given the use of an optimized M16C/28 architecture for a compute intensive task. The second being the unique ability to maintain network connectivity in the face of severe power depletion of the Co-S module, which can be shut down separately on-the-fly by the host controller. The host module can continue to communicate with the rest of the sensor network even in the face of this extreme situation. This unique ability to allow the Co-S to shut down and yet maintain network connectivity is apposite for reliability concerns.

2.2 Storage Architecture

The humongous amount of onboard flash storage is most suitable for long term data retention, as well as data sampled at fast sampling rates. Storing data generated from such sensors as audio circuits, necessitate high-capacity storage on the sensor platform. The energy required for the transmitting one byte is roughly equivalent to executing 688 CPU instructions, and the cost of writing to the flash is less than 10% of the energy required to transmit the same amount of data [3], thus making local storage and processing highly desirable. The Sense-and-Store paradigm pivots on this very observation. Since the wireless interface is unable to keep up with the high sampling rate of the sensor it is but logical to store the data onto onboard storage, and calculate required features in-situ. On a 1GB SD-Card we may store more three years worth of sensed data, continuously sampled at a rate of ten bytes per second, which more than suffices the demands of a wide spectrum of sensor applications. The data transfer mechanism to and from the Co-S platform is the SPI bus. The flash memories are powered off the Co-S platform. The microcontroller transfers data using the SPI protocol. Each write transaction to the SD-Card involves writing a 512 byte block of data, while reads may be arbitrarily sized up to a maximum of 512 bytes. The suitability of employing the SNA architecture Co-S platform is demonstrated by its efficient architecture, which is indicated by the performance metrics obtained by running the 128point FFT benchmark. The higher throughput, of the Co-S architecture enables faster data processing upto **24** times that of the Atmel AVR architecture (MICA) or the HP only. Additionally a **29%** improvement in power efficiency tilts the scales unambiguously in favor of the SNA. The low power consumption of the Co-S module results in savings upto **6uJ** per 128 point FFT operation when compared to the Stargate (Intel PXA 255).

3. CONCLUSIONS

The Our research efforts has been able to bridge the two most behooved requirements of sensor platform design, namely power efficiency and increased computational capability via means of a new split-level sensor platform. Our architecture is not only faster than conventional sensor nodes deployed today, but is also extremely power efficient, flaunts gigabyte scale on-board memory and has an implicit failover support mechanism, due to its inherent design. Overall, a total thumbs up in terms of a better, more powerful and more efficient sensor platform.

4. REFERENCES

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