All-Digital Quadrature Modem for High Speed Wireless Communications

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References

- A VLSI Architecture for a High-Speed All-Digital Quadrature Modulator and Demodulator for Digital Radio Applications. ”Henry Samueli and Bennett C. Wong”, IEEE Journal on Selected Areas in Communications, Vol8, No 8, October ‘90
- A BPSK / QPSK Timing – Error Detector for Sampled Receivers. “Floyd M Gardner”, IEEE Transactions on Communications, Vol. COM-34, No 5, May ‘86
- A survey of CORDIC algorithms for FPGA based computers. “Ray Andraka”, FPGA 98, Monterey, CA, USA

Modem

- QPSK (Quadrature Phase Shift Keying)
- 10MHz Data rate
- IF at 10MHz
- Upto 40MHz Data rate
- Reconfigurable Devices (FPGA)
- Digital Filtering
- Digital Modulation and Demodulation
- Applications: Point to Point W/Less Links and Satellite Communications.

QPSK Modulation

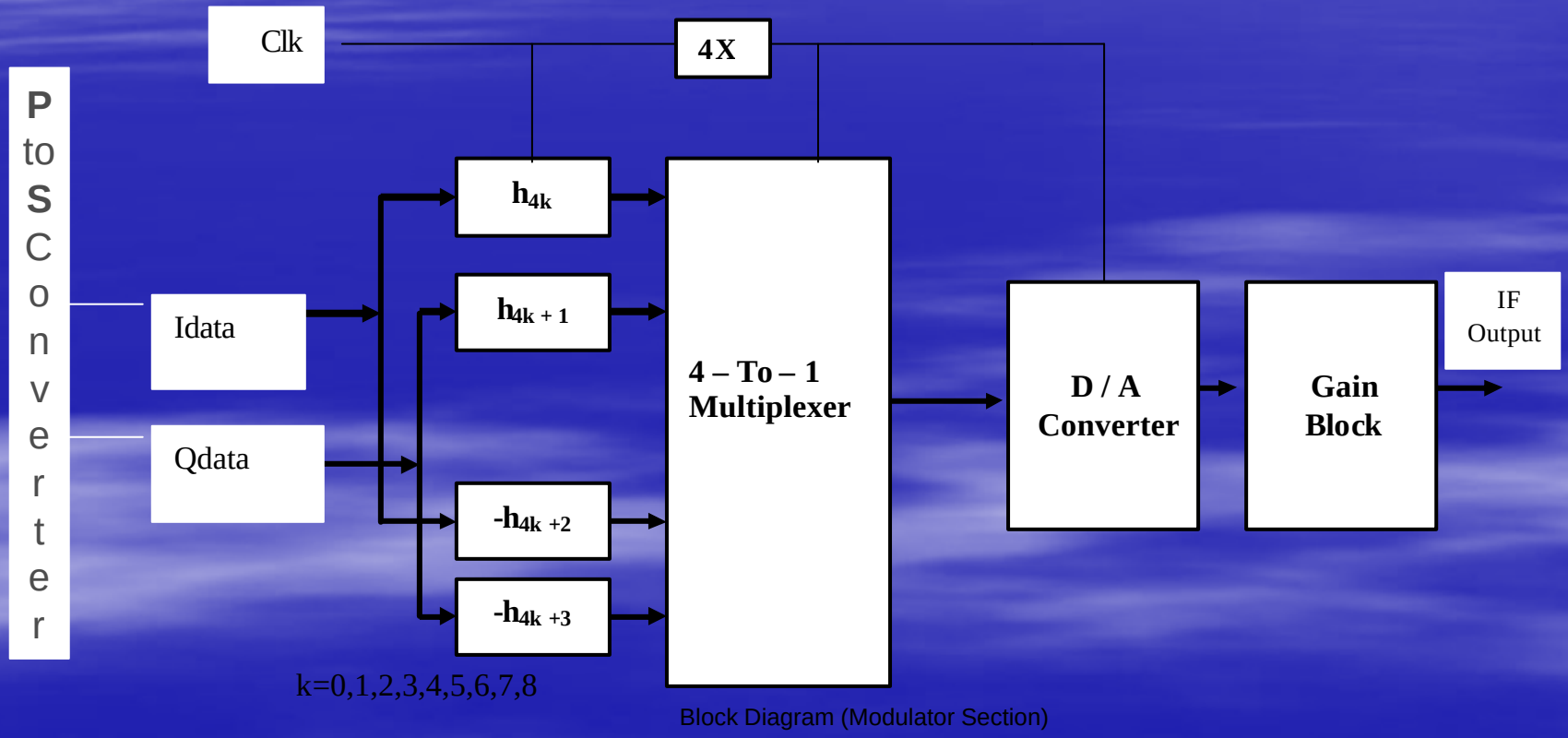
Input	(I) Mixer	(Q) Mixer	Sum	Sum (solved)
00	$-\sin wct$	$-\cos wct$	$-\sin wct - \cos wct$	$\sin(wct - 135°)$
01	$-\sin wct$	$\cos wct$	$-\sin wct + \cos wct$	$\sin(wct + 135°)$
10	$\sin wct$	$-\cos wct$	$\sin wct - \cos wct$	$\sin(wct - 45°)$
11	$\sin wct$	$\cos wct$	$\sin wct + \cos wct$	$\sin(wct + 45°)$

Waveform	Sample Tn	Sample Tn+1	Sample Tn+2	Sample Tn+3
Sine (Q)	0	1	0	-1
Cosine (I)	1	0	-1	0

Modulator

- 32 bit RRC filtering
- IF at 10MHz
- Analog LPF with B/W 13MHz
- 10bit precision digital output
- Parallel multiplication (LUT based)
- When I carrier is sampled ‘1’ or ‘-1’, the Q carrier is sampled ‘0’ which means at any sampling instant we need to process only one of the carrier.
- PRBS Generator used to generate Random Sequence

Modulator



Block Diagram (Modulator Section)

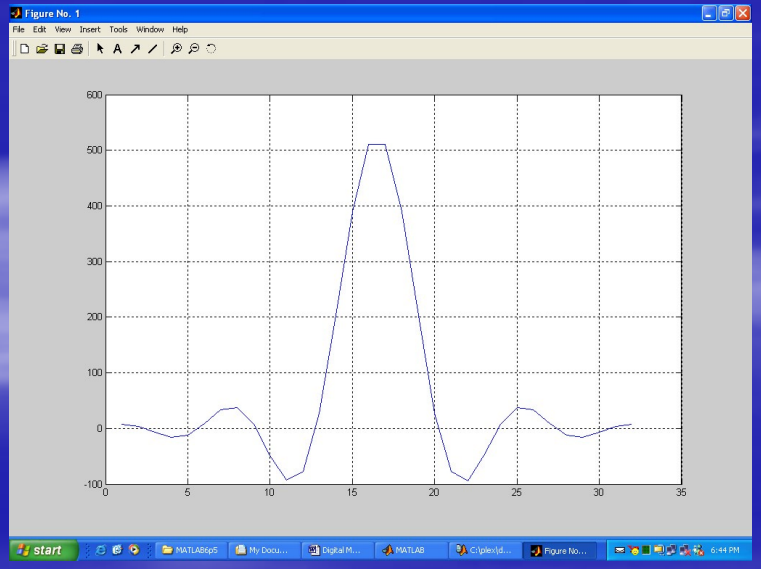
Digital Filter

- Root Raised Cosine (Low Pass)
- Avoids ISI
- Digital Filter Coefficients:

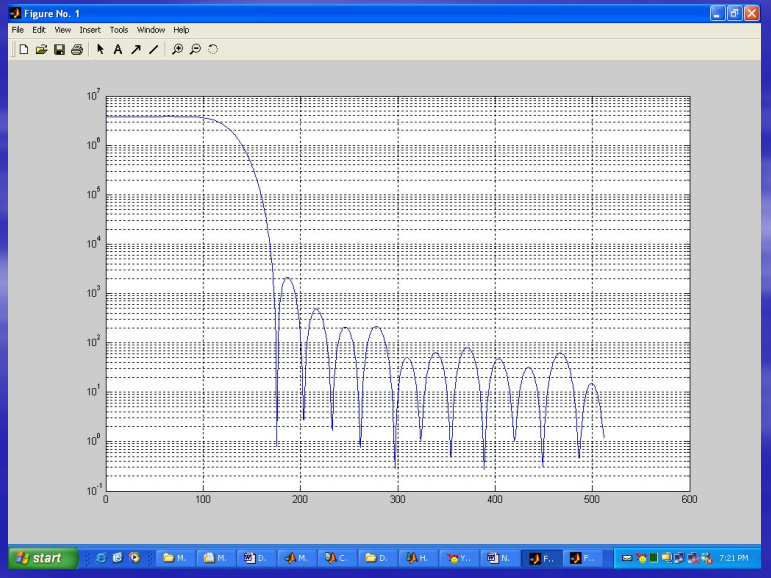
7 4 -7 -16 -12 9 33 38 8 -48 -93 -77 27 203 390 511

511 390 203 27 -77 -94 -48 8 38 33 9 -12 -16 -7 4 7

- Transmit filter has to meet the following specifications:
- Operating Frequency : 10 MHz.
- No. of Taps : 32
- Roll of factor ? : 0.3
- Pass band Bandwidth : 13 MHz

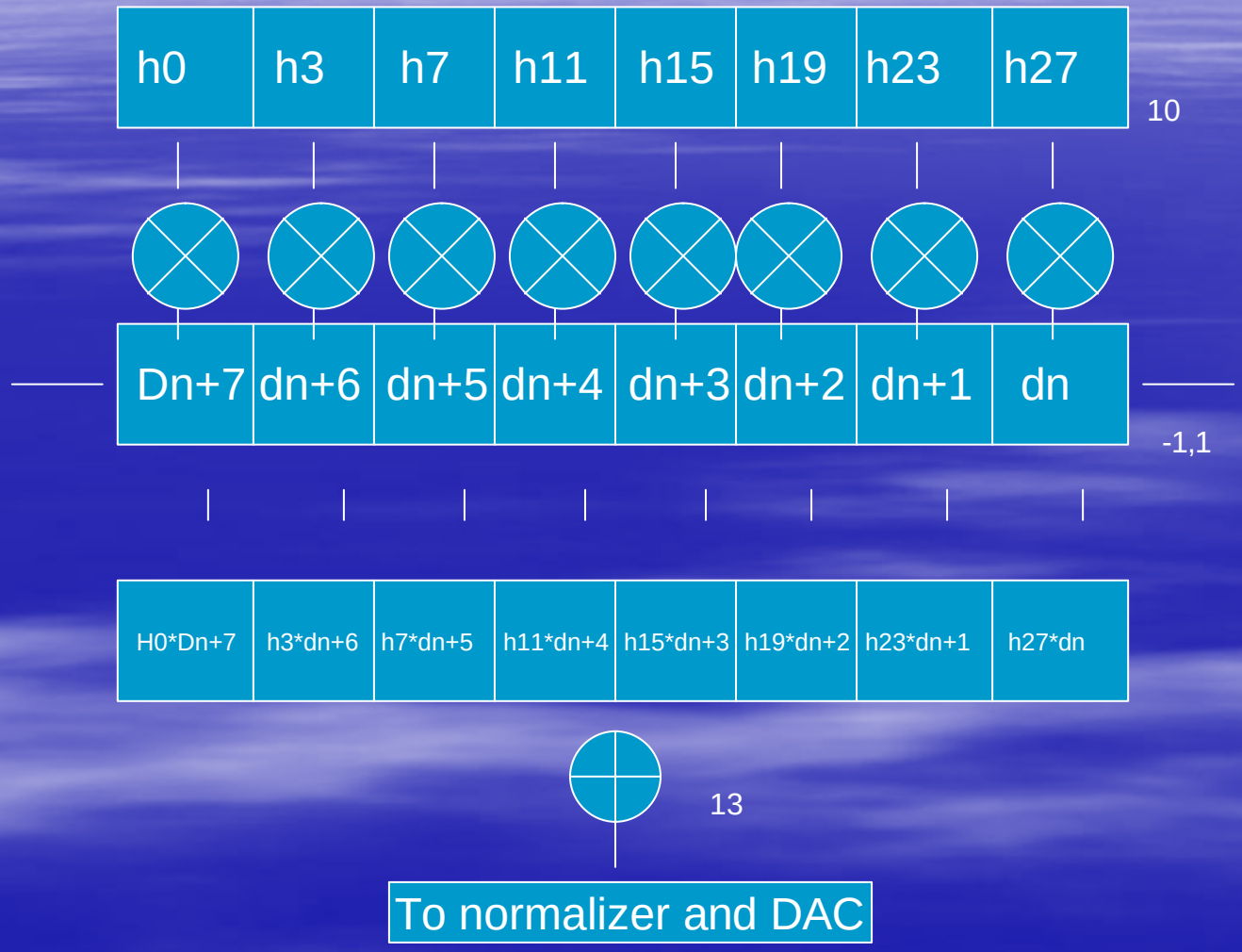


Impulse Response

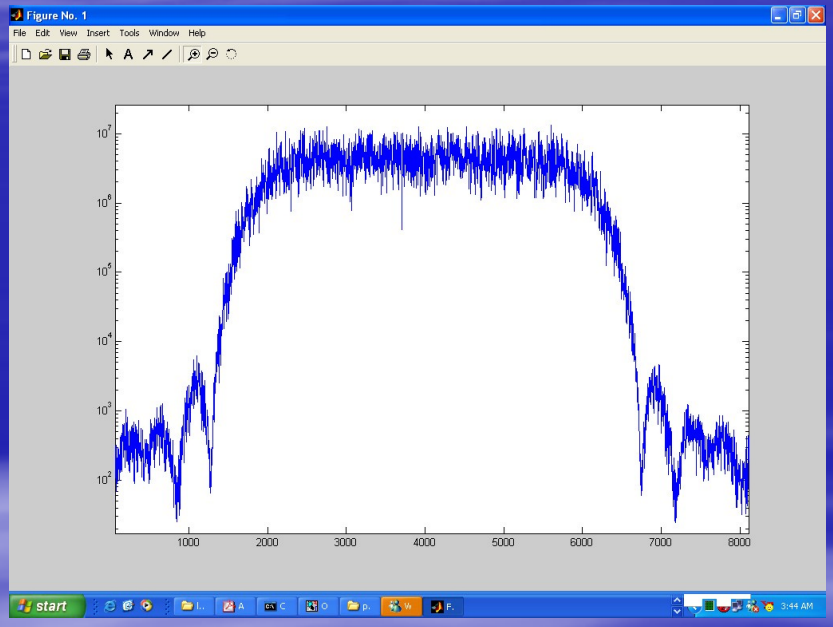


Frequency Response

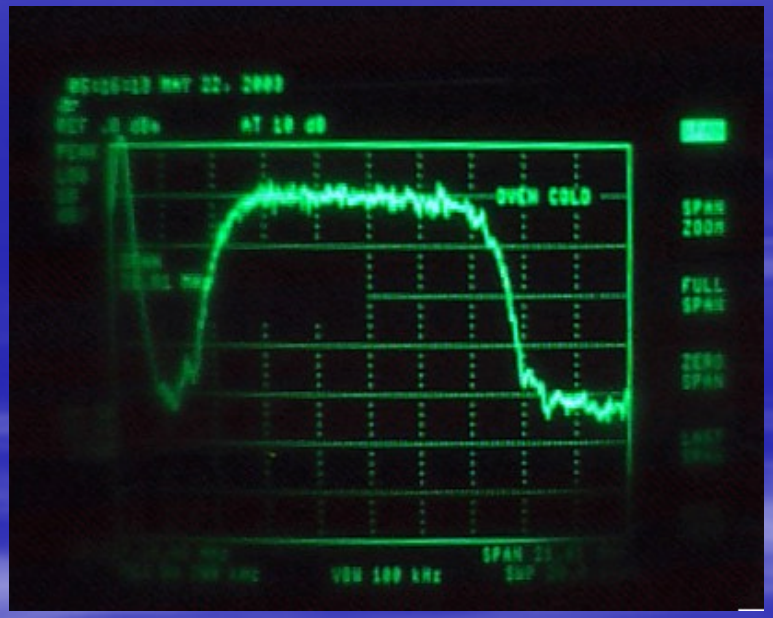
Tx Sub Filter



Transmit Spectrum



Simulated, 10 MHz

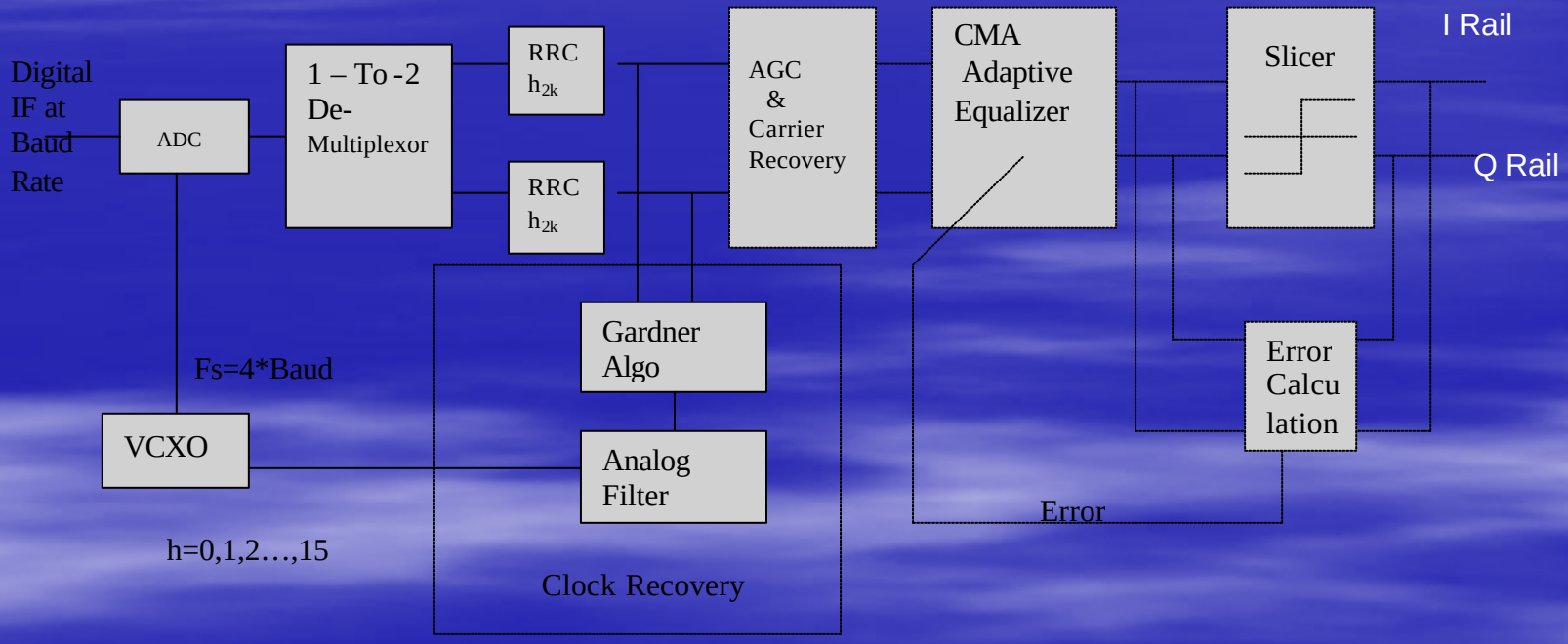


Actual, 10MHz

Demodulator

- 10MHz IF, sampling rate = 40MHz
- 32 bit RRC Filter
- 16bit I,Q rail subfilters, clocked at 20MHz
- Automatic Gain Control
- Demodulation = De-Multiplexing and Inversion Control
- Timing Recovery
- Carrier Recover
- CMA Equalizer

Demodulator Block Diagram



Receiver Block Diagram

Rx Sub Filter (pipelined)

Ambiguities

- Clock Ambiguity
- Carrier Ambiguity
- Polarity Ambiguity
- I / Q Channel Ambiguity
- Resolving

  Clock Recovery

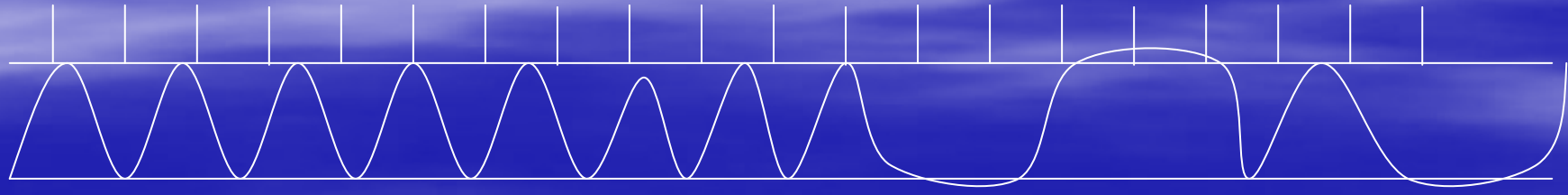
  Carrier Recovery / Derotation

  Differential Encoding

  Internal Channel Selector

Clock Recovery

- Garderner's Zero Crossing Detector
- $e(n) = I(n-1/2)[I(n) - I(n-1)] + Q(n-1/2)[Q(n) - Q(n-1)]$
- Error = Sum of both I and Q channels
- 10 bit digital error output converted to analog
- Error signal is used to control the VCXO



Carrier Recovery

- Carrier ambiguities result in a rotating constellation
- De-rotation is needed
- Using CORDIC algorithms (iterative algorithm for coordinate rotation)
- If the rotation angle is limited to tan(2^{-i}) then multiplication by tangent term becomes a shift operation.
- The final equation results in

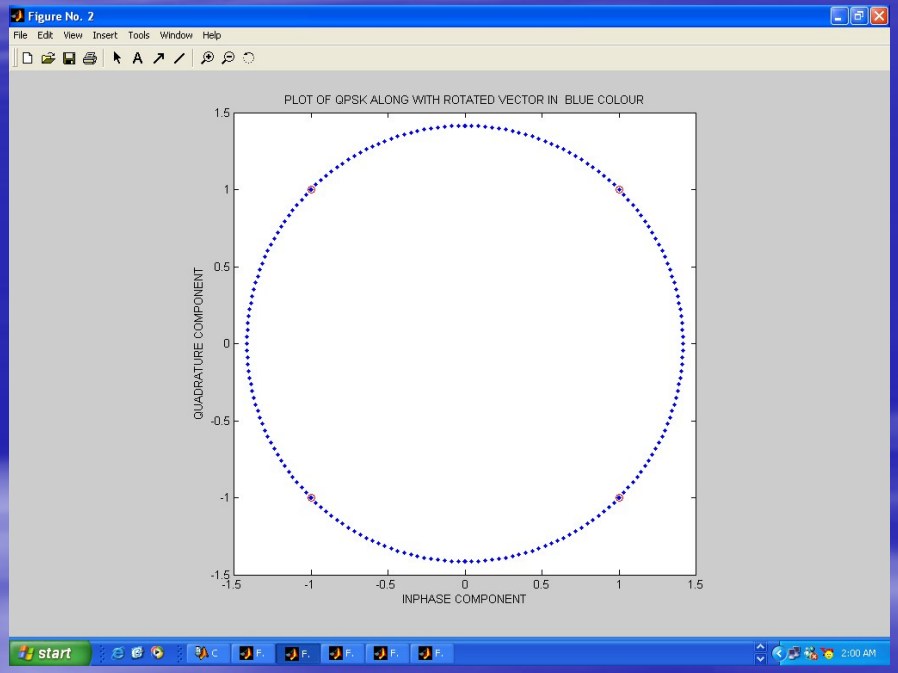
$$X' = \cos f [X - Y \tan f]$$

$$Y' = \cos f [Y + X \tan f]$$

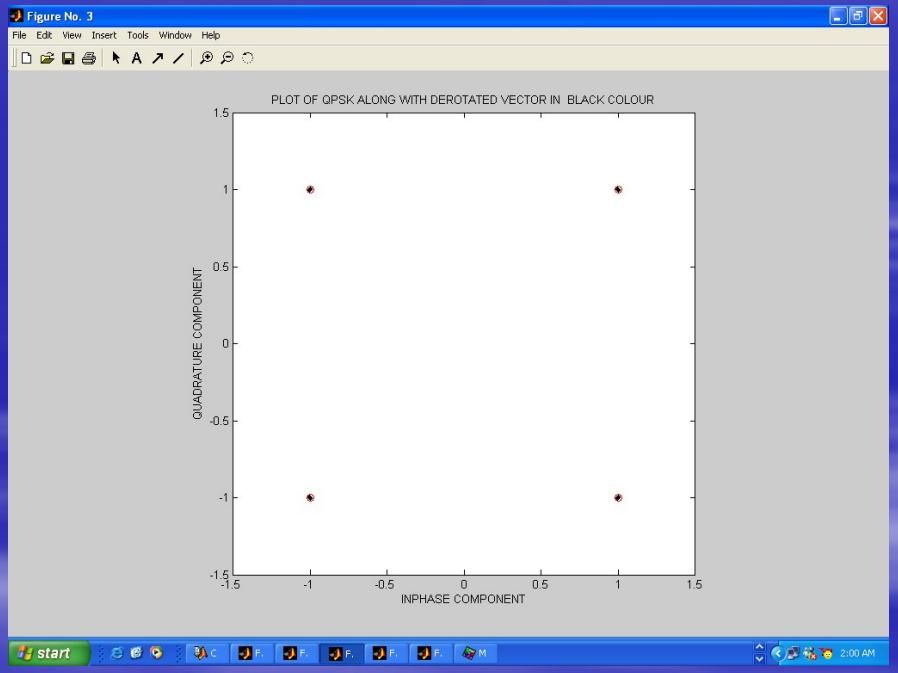
$$Xi + 1 = Ki[Xi - Yi.di.2^{-i}]$$

$$Yi + 1 = Ki[Yi + Xi.di.2^{-i}]$$

Carrier Recovery



Before



After

CMA Equalizer

- Iterative Algorithm, Step size = 2
- The algorithm fits the constellation points to a circle of constant magnitude.
- Dependent on the accuracy of the AGC
- Decision directed algorithm
- C=C+cmaerror
- Cma error = (Radius CMA)^2 – (Radius C)^2

FPGA

- Reprogrammable Digital Hardware
- Extremely Customizable and parallel execution
- Very fast speed (150 MHz)
- Very low design turnaround time
- Simulation / Synthesis Tools
- Testing, Debugging, and Implementation
- XC 2S 200 (200 K system gates)
- XC 2V 1500 (1.5 M system gates)

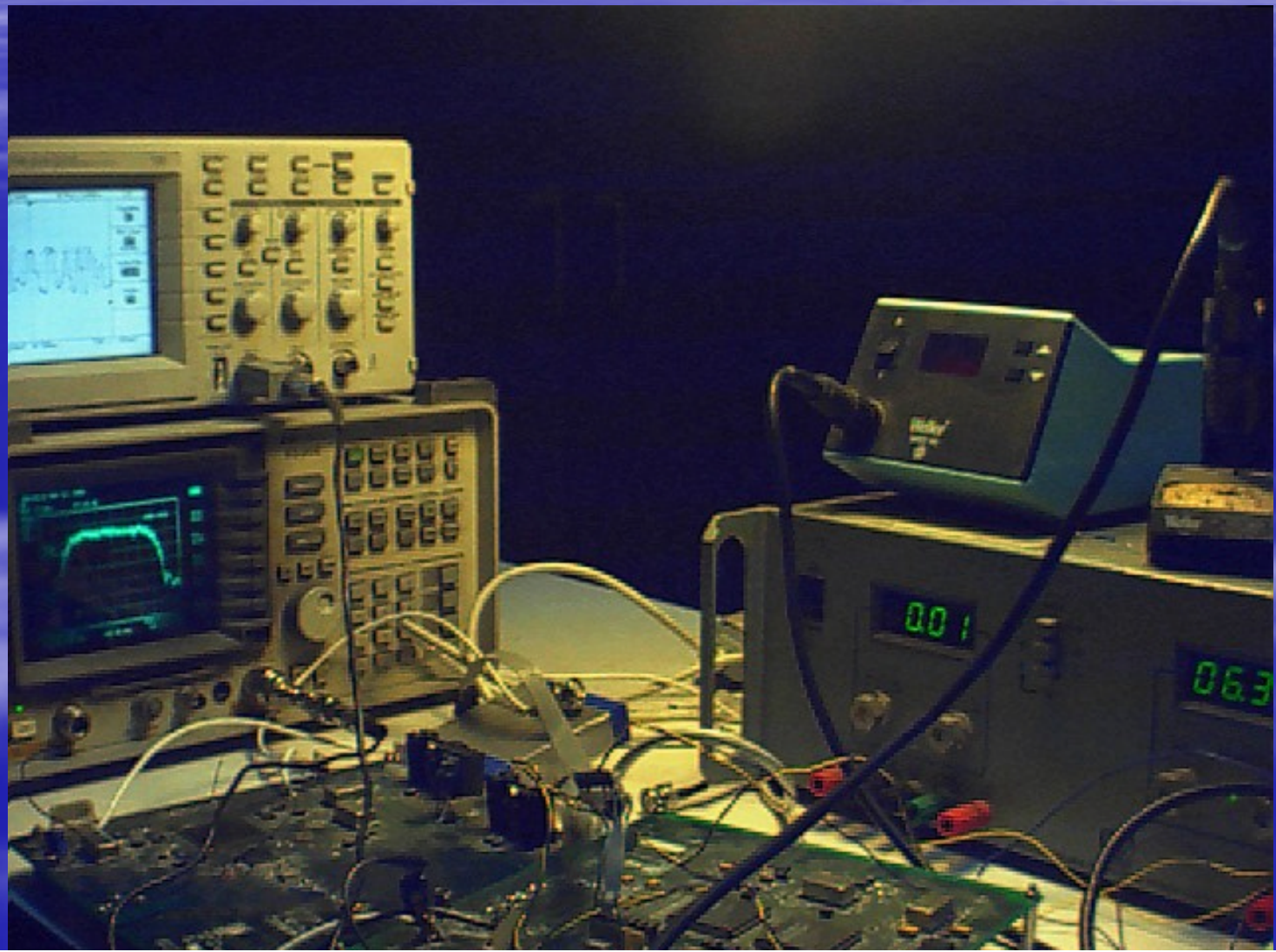
Implementation

- Quadrature Modulator (Tested)
- Quadrature Demodulator (Tested)
- PRBS generator (24 bit Maximal Length)
- Digital Filters
  Parallel Execution (Tx) (Tested)
  Pipelined Execution (Rx) (Tested)
- Timing Recovery (Tested)
- Carrier Recovery (Under Test)
- CMA Equalizer (Under Test)

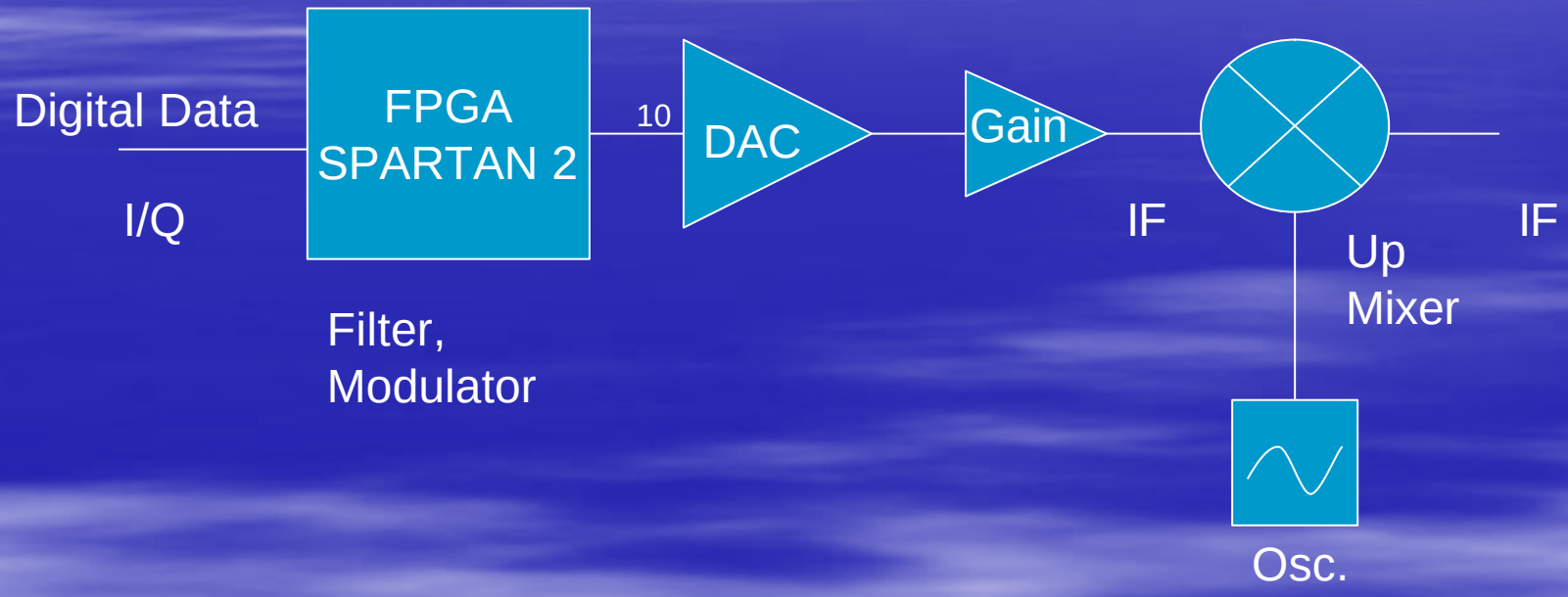
Test Bench

- Spectrum Analyzer
- Oscilloscope
- Personal Computer
- Xilinx ISE
- ModelSim Simulator
- MATLAB
- Modulator Board
- Demodulator Board

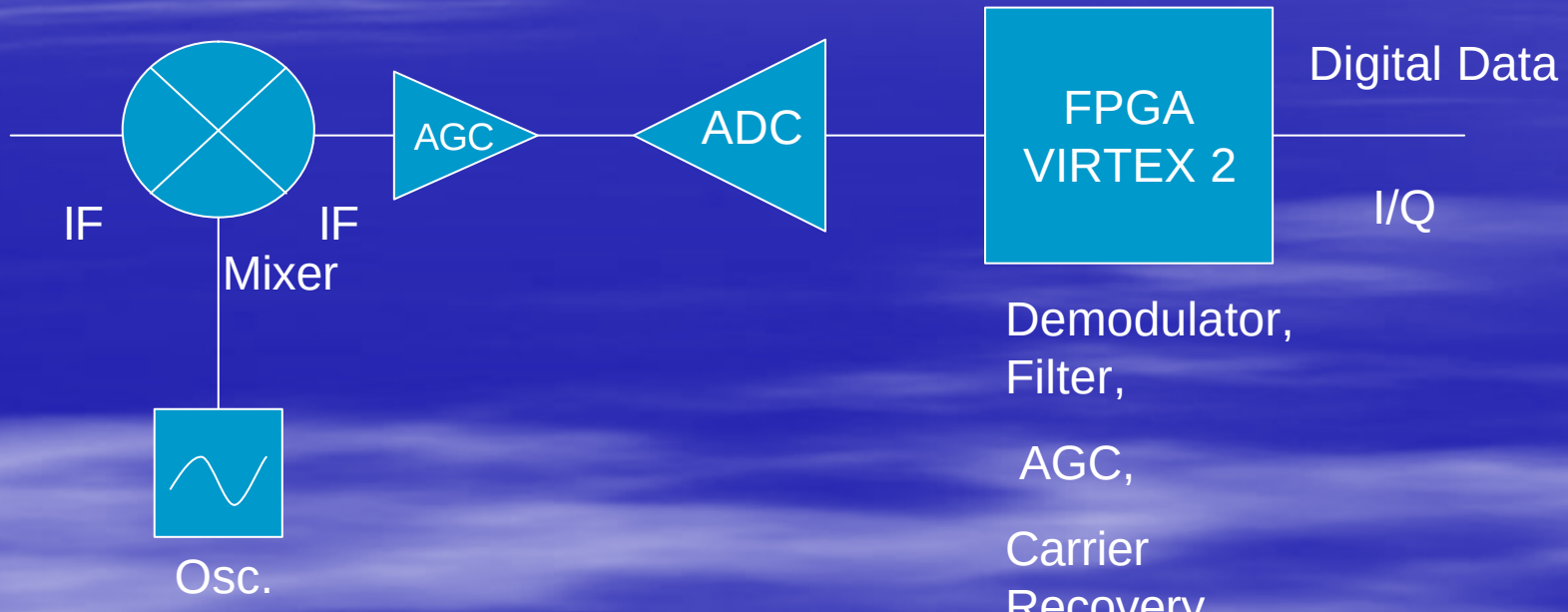
Test Setup



Transmitter



Receiver



Demodulator,
Filter,

AGC,

Carrier
Recovery

Clock
Recovery

CMA
Equalizer

Clock Recovery