

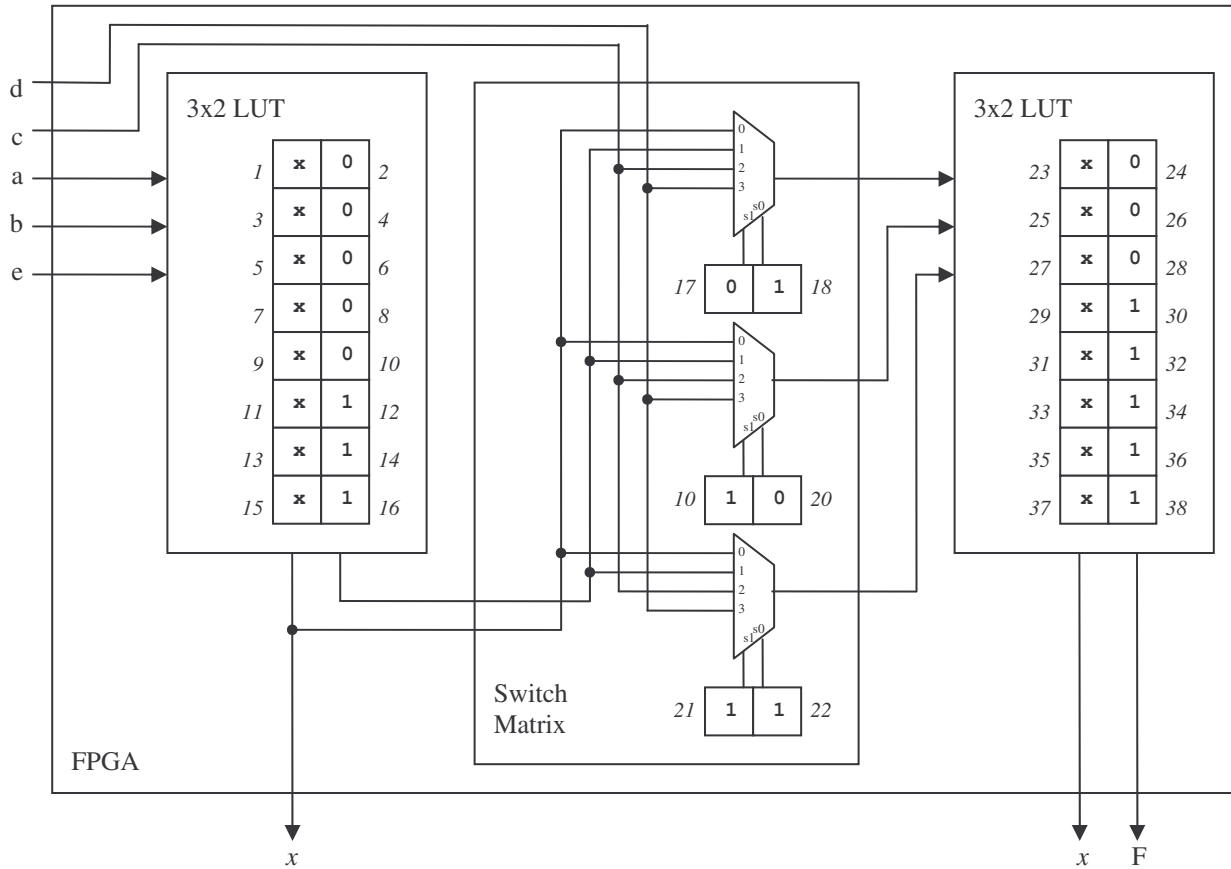
UCR CS122A, Fall 2005
Prof. Frank Vahid
Homework 3

Working in groups is encouraged. 10% extra credit for groups of 3 or more working together for an hour or more. Write down each others' names, and when/where you met. Every student should still solve every problem and submit his/her own solutions; working together is useful to understand the problems, discuss solution ideas, and compare answers.

You can choose to submit this homework electronically (as a single file, submitted to the department's server), or on paper. Expected time is 3-4 hours -- please record and report your actual time per problem. Start early!

1. Design your own FPGA. The specifications for your FPGA are:
 - * The chip should have 5 inputs and 3 outputs.
 - * The fabric should consist of 3-input 2-output lookup tables (LUTs). You need NOT create configurable logic blocks (CLBs), which have flip-flops too -- your FPGA will only support combinational logic.
 - * The fabric should include switch matrices (SMs).
 - * The fabric should be sufficient to implement the circuits specified in the subsequent problem.

Show the internal design of your LUT and your SM, using memories, gates, decoders, muxes, and other standard components as building blocks. All your LUTs and SMs should be identical internally, so you need only show the internals of one of each. Also show the overall architecture, consisting of all your LUTs and SMs and their interconnections with each other and external pins. You do NOT need to specifically implement your scan chain in your LUT/SM internal designs, but you should clearly indicate which components are part of the scan chain and in what order they appear in that chain.

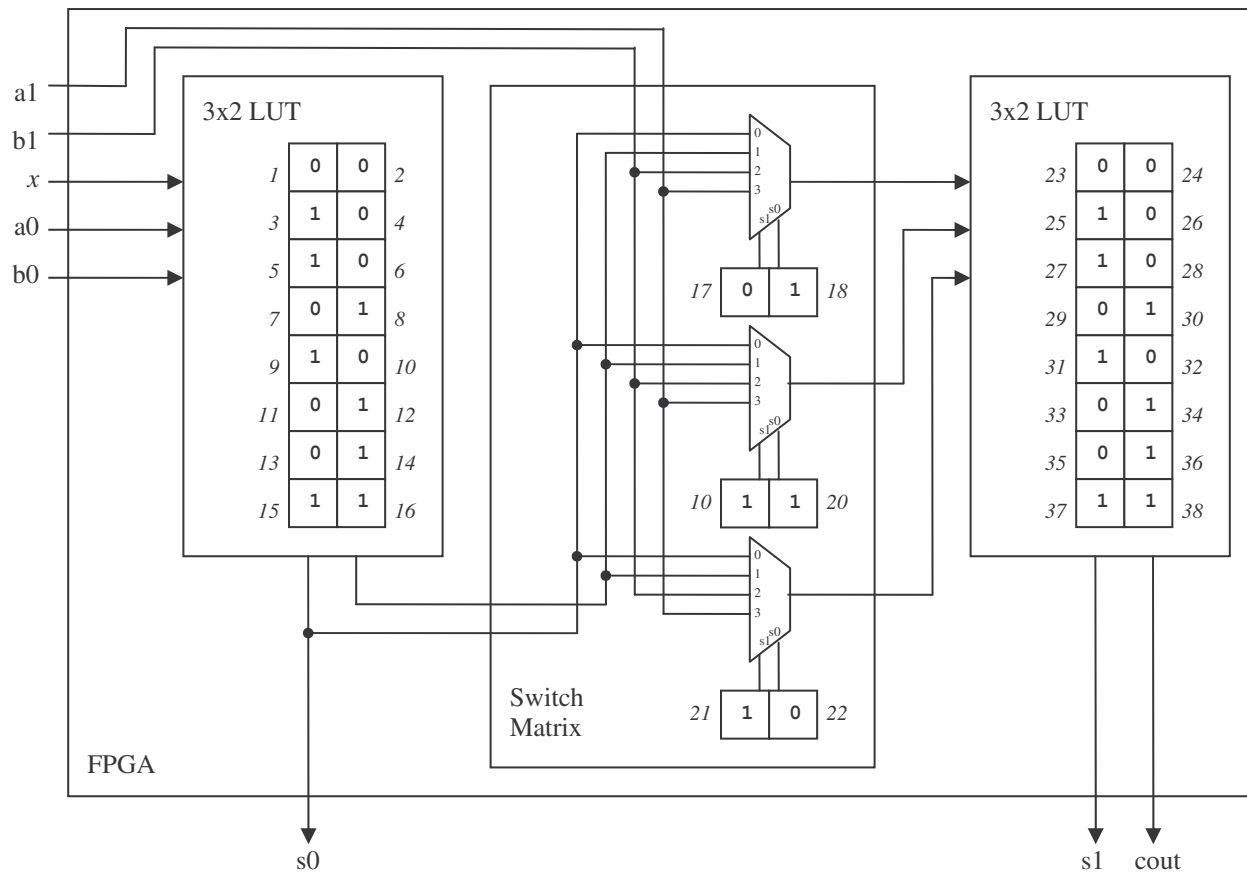


The corresponding bitstream is:

x0x0x0x0x0x0x1x1x1 011011 x0x0x0x1x1x1x1x1

(b) Implement a 2-bit carry-ripple adder: $a_1 a_0$ PLUS $b_1 b_0 = \text{cout } s_1 s_0$.

| | | | | | | | | | | |
|------------|---|----|----|----|----|----|----|----|----|------|
| c0 | x | a0 | b0 | s0 | c0 | c0 | a1 | b1 | s1 | cout |
| a1 a0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| + b1 b0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| ----- | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| cout s1 s0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |



The corresponding bitstream is:
 0010100110010111 011110 0010100110010111

A note on working together -- the odds of coming up with identical or even very similar fabrics are very low. You should each create your own fabric. Working together is a way to help each other when stuck, explain concepts, etc. But each person should do his/her own FPGA design.